DEVELOPMENT OF AN IMPROVED FORCED ISLAND AND LOAD SHEDDING SCHEME TO PREVENT SYSTEM COLLAPSE

BY

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DEPARTMENT OF ELECTRICAL ENGINEERING

FACULTY OF ENGINEERING

AHMADU BELLO UNIVERSITY ZARIA, NIGERIA

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DEPARTMENT OF ELECTRICAL ENGINEERING

FACULTY OF ENGINEERING

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NIGERIA

MAY, 2018

DECLARATION

I declare that the work in this dissertation entitled "DEVELOPMENT OF AN IMPROVED FORCED ISLAND AND LOAD SHEDDING SCHEME TO PREVENT SYSTEM COLLAPSE" has been carried out by me in the Department of Electrical Engineering. The information derived from literatures has been duly acknowledged in the text and a list of references provided. No part of this dissertation was previously presented for another degree or diploma at this or any other institution.

Yakubu Sale Gelta _____ _____

Signature Date

CERTIFICATION

This Dissertation entitled "DEVELOPMENT OF AN IMPROVED FORCED ISLAND AND LOAD SHEDDING SCHEME TO PREVENT SYSTEM COLLAPSE'' by YAKUBU Sale Gelta meets the regulations governing the award of degree of Master of Science (MSc) in Power System Engineering of the Ahmadu Bello University, and is approved for its contribution to knowledge and literary presentation.

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DEDICATION

This research work is dedicated to my parents and siblings**.**

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ABSTRACT

This research work presents a scheme that identifies line outage and generator outage using contigency analysis and effectively splits the network into a set of predefined islands, with a load shedding strategy to minimise the adverse effect of each outage and to ensure system security. In this research work, Newton Raphson power flow was used for the power flow analysis of the network. Also, Active Power Loading Perfomance Index was used during the contigency analysis to rank the transmission line and generator outage based on the severity of each outage. For each outage causing a line overload and voltage violation, the network splits into predefined islands and power flow analysis is performed on the new island to check the stability of the network. For each island found to be unstable, a power mismatch, and under voltage load shedding scheme is used to ensure the system stability. The developed algorithm was implemented on the IEEE 6 and 14 test bus network. From the IEEE 6 bus network, ten outages resulted in the split of the network into two islands. Also, the developed load shedding scheme was applied on each island that was found to be unstable after power flow analysis. The average voltage profile improvement of the island network over the base case was found to be 13.02% after load shed of 42.3 MW. Also, from the IEEE 14 bus network, the contigency analysis considered twenty four outage, with twenty one outage causing a split of the network into two islands. Load shedding scheme was also applied on each newly formed island found to be unstable. The average voltage profile improvement of the islands over the base case was 2.89% after load shed of 80.92 MW. The validation of this research work was performed by simulation, and comparing with the work of Soman *et al*,.(2015a), using load shed speed and voltage profile as performance metrics. The developed method obtained an average load shed speed improvement of 63.3% and an average voltage profile improvement of 1.01%. Also, from the results obtained, it is quite evident that the developed scheme has a better performance than Soman *et al*,.(2015a).

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LIST OF ACRONYM

ACRONYMS	DEFINITION
AC	Alternating Current
APLPI	Active Power Loading Performance Index
DC	Direct Current
EPS	Electric Power System
IEEE	Institute of Electrical Electronics Engineering
LS	Load Shedding
MATLAB	Matrix Laboratory
MVAr	Mega Voltage Ampere Reactive
MW	Mega Watt
NERC	North American Electric Reliability Corporatio
NRLF	Newton Raphson Load Flow
PM	Power Mismatch
PQ	Active and Reactive Power
p.u.	Per Unit
PV	Active Power and Voltage
R/X	Resistance/ Reactance
UVLS	Under Voltage Load Shedding

CHAPTER ONE

INTRODUCTION

1.1 Background of Study

Power system networks mostly operate close to their stability limits as a consequence of the deregulated electricity market, growth in energy consumption and lack of expansion of transmission networks due to economic and environmental constraints. Under such operating conditions, a severe disturbance such as a loss of generating units or faults along transmission lines may lead to cascading events. Thus, the risk of collapse and blackout of the overall power system is increased (Tang *et al.*, 2013). Security of a power system refers to the degree of risk in its ability to survive imminent disturbances (contingencies) without interruption of customer service. It relates to robustness of the system to imminent disturbances, and hence depends on the system operating condition as well as the contingent probability of disturbances. Electric power system security analysis encompasses three functions namely system monitoring, contingency analysis and corrective control in which safe island formation and load shedding are some of the corrective control (Ezhilarasi & Swarup, 2009). Power system blackout is the state when partial or complete areas of the system collapse due to cascading of failure events which causes mass scale tripping of transmission lines and generating units (Soman *et al.*, 2015a). Islanding (also known as loss of grid or Loss-of-Mains – LoM) represents "a condition in that a portion of the power system that contains both load and generation remains energized while isolated from the remainder of the power system". An island represents a condition where a portion of an area electric power system (EPS) is energized solely by one or more local power sources while that portion of the area EPS is electrically separated from the rest of the area EPS. Islanding appears when some part of the utility grid loses connection with the rest of the system (Banu & Istrate, 2014). Controlled islanding

is a critical way of preventing large disturbances from propagating into the rest of the system and causing a severe breakup and blackout. In a system, more islands will lead to longer resynchronization times, and cutting more interconnections between the islands would have higher risks of introducing disturbances into the system. Thus the smallest number of islands which is ideally two should be the best islanding scheme (Lin *et al.*, 2014). The technical issues in achieving safe and smooth operation of islanded events are speed governor response, range of operating power, voltage and frequency control, earthing or equivalent protection of the island operation, and resynchronisation to the grid. Among these technical issues, voltage and frequency control tends to occur more frequently, of which load shedding is considered the most effective technique to overcome the problem. The only means of stabilizing the voltage and frequency to their nominal values in an islanded system is by rejecting several loads through a load shedding scheme (Khamis *et al.*, 2015). Under Voltage Load Shedding is based on the possibility of disconnecting some loads (or percentage of load) after a severe contingency, in order to relocate the operating point far from the critical value (López *et al.*, 2016). To prevent system failure during extreme emergencies, it is recommended to execute controlled splitting of the system into stable islands with generation and load shedding schemes. Such formed islands are more stable than unintentionally formed islands and are less prone to reach conditions that lead to total blackout of the entire system (Soman *et al.*, 2015d). One of the most important factors in the operation of any power system is the desire to maintain system availability and reliability. This ensures a secure operation of the system and improved economic operation. Power system security is the ability of the system to withstand one or more component outages with the minimal disruption of service or its quality (Nnonyelu *et al.*, 2014). In large disturbances of power system, usually frequency decays are accompanied with voltage decays at load buses which reduce the system security, so to restore a system due to

frequency decline actual levels of load shed by under frequency load shedding (UFLS) or under voltage load shedding (UVLS) are relative to the levels required and expected, this required levels are calculated using power system analysis (Balasubramaniam *et al.*, 2016; Moafi *et al.*, 2016). In addition, active power deficit is usually accompanied by a reactive power deficit. This reactive power deficit results in a sudden decrease in the voltage of all the buses which in turn requires some of the loads that decreases the frequency to be dropped (Marzband *et al.*, 2016).

Load shedding is an emergency control action to ensure system stability, by curtailing system loads, this action only takes place when system frequency/voltage falls below a specified threshold. Typically, the load shedding attempts to balance real and reactive power supply and demand in the system (Bevrani *et al.*, 2010). Power system experience severe voltage and frequency disturbance due to the imbalance between the generation and load after islanding occurs. The frequency/voltage rapidly decreases which may be damaging to rotating machines and other load equipment within the island, and it will be essential that certain amount of load be shed to restore system frequency/voltage to nominal value in order to prevent total system collapse (Laghari *et al.*, 2015). When an extreme failure event occurs in a network, under voltage load shedding can be applied as an economical method for preventing voltage collapse in order to maximize the power system loadability (Majidi *et al.*, 2014). An undervoltage load shedding scheme should address two tasks: the detection of voltage instability following a large disturbance and the determination of the amount of load to be shed. In case of short term voltage instability, the scheme should be fast (Damodhar & Krishna, 2016).

Due to the economic challenges associated with blackouts, researchers have proposed schemes to help identify outage which could lead to system collapse. Dola and Chowdhury (2006) proposed a blackout mitigation technique based on strategic tripping of overloads. Nnonyelu *et al.*, (2014)

presented a reliability evaluation analysis considering system line overload index (SLOI) for contingency ranking but not considering generator outage. Li *et al.*, (2014) developed a zone division scheme based on sensitivity analysis by lumping up buses for its analysis. Soman *et al.* (2015a) presented an algorithm that identifies the risk during an outage and forcefully splits the system into predefined islands using DC power flow for its system analysis. Therefore, this research work proposes an improved scheme considering generation and transmission line outage for its contingency analysis, the use of Newton Raphson load flow for accuracy, and an optimum load shedding strategy to balance generation and load considering power imbalance, voltage deviation and thermal limit constraints.

1.2 Motivation

During the planning and operation of a power system, there is need for corrective control to severe contingencies in order to ensure steady power delivery to loads. Contingencies such as generator and line outage could cause voltage violation, and line limit violation which could lead to total system collapse. Thus, a need for accurate forced island formation to prevent cascading of fault, and a fast load shedding scheme as a corrective control is of importance, and a motivation for this research work.

1.3 Significance of Research

The significance of this research is the development of an improved forced island and optimal load shedding scheme to prevent total system collapse in the event of line outage and generator outage contingencies considering power imbalance, bus voltage magnitude, line maximum loading, and time to stability for the load shedding scheme. Previous researchers did not consider the use of this scheme to prevent total system collapse.

1.4 Statement of Problem

Power system contingencies (line, transformer, generator outage) cause redistribution of power flow and violation of line and bus voltage limits, which leads to cascade failure and collapse of the entire system. The problem related to load shedding and islanding scheme is the development of a strategy to define the location, and amount of load to shed for every severe faults in order to save the system from total collapse. This research work developed a scheme for predefined island formation and optimal load shedding scheme to ensure continious supply to customers and prevent cascade failure which leads to total system collapse.

1.5 Aim and Objectives

The aim of this research is to develop improved forced island and load shedding scheme to prevent total system collapse. In order to achieve this aim, the following are objectives of the study:

1. To perform a power flow analysis using Newton Raphson power flow technique.
2. Develop a forced island and optimal load shedding scheme based on power system contingency analysis.
3. Validation by comparing the developed scheme with the work of Soman *et al.*, (2015a),

1.6 Dissertation Outline

The introduction to this research has been presented in Chapter One. Detail review of related literatures and relevant fundamental concepts, and review of similar works published, related to this research is contained in Chapter Two. Chapter Three presents the methodology and materials used. The results obtained after applying the improved methods on the IEEE 6 bus, and also the performance of the developed scheme on IEEE 14 bus is presented in Chapter Four. Chapter Five presents conclusion, and recommendations for further work. While list of cited work, data and MATLAB codes are given in the appendix section provided at the end of this research report.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

In carrying out the research, some literatures were reviewed, which serves as a guide towards achieving the set goals. The review of these relevant literatures is categorized in two parts: Review of fundamental concepts, and Review of similar works, which are further discussed.

2.2 Overview of Fundamental Concept

Some of the fundamental concepts regarding the research work are discussed. These concepts served as background to the study.

2.2.1 Power System Background

Electric power system is a complex network consisting of equipment like generators, transformers, transmission lines, and loads. The primary function of transmission is to transmit bulk power from sources of desirable generation to bulk power delivery points. On the other hand, distribution system is mainly responsible for the conveyance of power to the consumer by means of lower voltage network (Gonen, 2011). The electricity required to meet consumption needs is generated in production centers commonly called power plants or stations, where a source of primary energy is converted into electric power with clearly defined characteristics. Specifically, these facilities generate a three-phase, sinusoidal voltage system, with a strictly standardized and controlled wave frequency and amplitude (Gómez-Expósito *et al.*, 2016).

2.2.2 Power system blackout

A blackout in a power system refers to the unavailability of electric power in an area for a short or long duration. These power blackouts can occur due to natural reasons as well as technical reasons. Natural reasons include animal contact with a live conductor, a vehicular accident resulting in

damaged transmission poles, and trees falling on transmission lines due to stormy weather. Technical reasons include faults, damaged transmission or distribution lines, stability issues, overloaded transmission lines, cascading events, faulty equipment. The estimated unsupplied energy is another important factor leading to blackouts (Laghari *et al.*, 2013). Some of these reasons, like faults, are initiating contingencies; others are the subsequent consequences of those events which may result in instability and cascading, leading to a blackout.

The social impact of a power blackout, especially in urban areas, is severe – health care facilities in hospitals are affected, traffic control problems lead to accidents, and the Internet and other communications systems break down. The detailed consequences of power blackouts are shown in Figure. 2.1

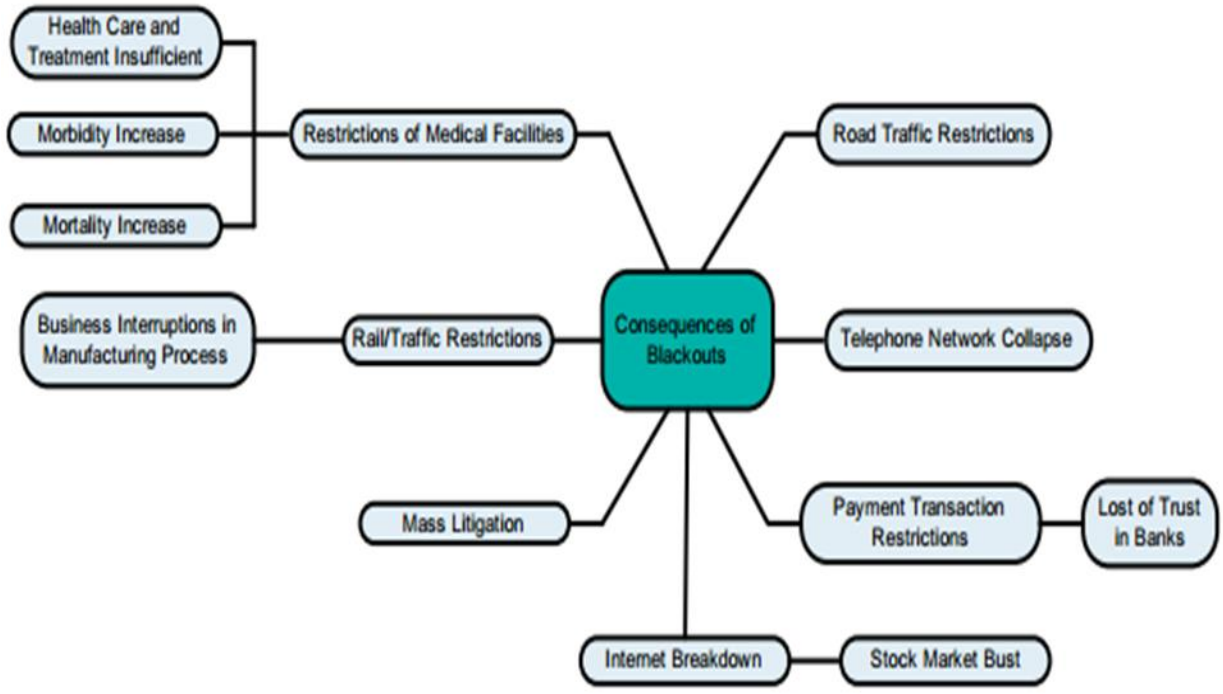


Figure 2.1: Consequences of power blackouts (Laghari *et al.*, 2013)

2.2.2.1 Voltage stability

Voltage stability refers to the ability of a power system to maintain steady acceptable voltages at all buses in the system after being subjected to a disturbance from a given initial operating

condition. It depends on the ability to maintain/restore equilibrium between load demand and load supply from the power system. A system is voltage unstable if for at least one bus in the system, the bus voltage magnitude decreases as the reactive power injection at the same bus is increased. Instability that may result occurs in the form of a progressive fall or rise of voltages of some buses. A possible outcome of voltage instability is loss of load in an area, or tripping of transmission lines and other elements by their protective systems leading to cascading outages (Kundur *et al.*, 2004). The term *voltage collapse* is the process by which the sequence of events accompanying voltage instability leads to a blackout or abnormally low voltages in a significant part of the power system (Kundur *et al.*, 2004). Voltage collapse can be studied using power flow V-Q or P-V analysis, using voltage sensitive load modeling, and control action steps in sequences of power flow simulations (Shah *et al.*, 1999). Voltage stability studies are frequently undertaken through the use of static analysis. A common use of this is the development of P-V curve as shown in Figure 2.2

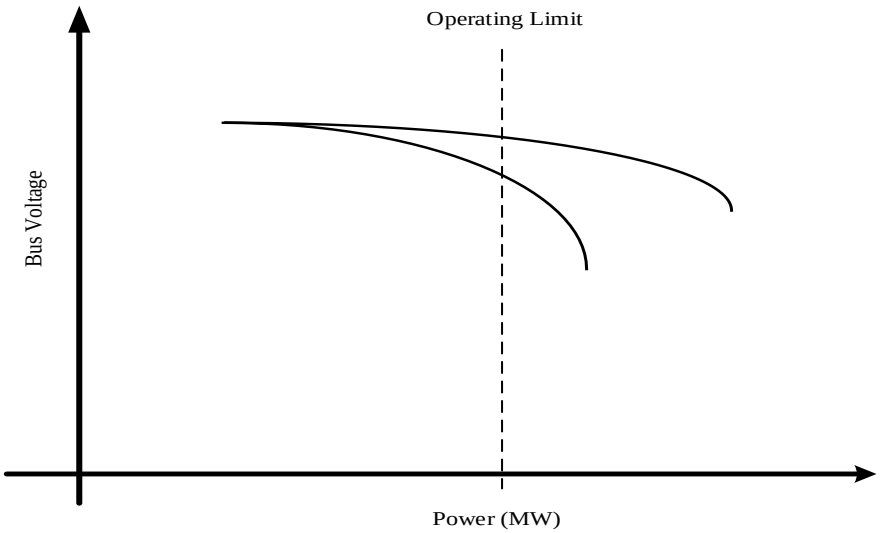


Figure 2.2: Power versus Voltage curve (Kundur *et al.*, 2004)

2.2.3 Transmission System

Most electricity generation takes place in large production centers scattered across a large geographical zone, at long distances from the major consumption centers. The transmission grid is responsible for carrying the electricity generated to the consumption centers, its key role in the dynamic equilibrium between production and consumption determines its typical web-like structure in which every station in the grid is backed up by all the others to avert the consequences of possible failures (Gómez-Expósito *et al.*, 2016). North American Electric Reliability Corporation (NERC) defines cascading as "the uncontrolled successive loss of system elements triggered by an incident at any location" (Dobson *et al.*, 2015).

2.2.3.1 Single phase representation of a balanced three phase system

The power system has three phases. These three phases can be either balanced or unbalanced. A balanced three phase network can easily be represented by a single phase equivalent circuit. This equivalent single phase circuit can be used to analyze the three phase system. The parameters (current, voltage, impedance, etc.) of the three phase network can be estimated using the single phase equivalent circuit (Das, 2007). Figure 2.3 shows a simple balanced three phase network. As the network is balanced, the neutral impedance Z_n does not affect the behavior of the network. Figure 2.4 gives the single phase equivalent of a balanced three phase network of Figure 2.3. As the system is balanced, the voltage and currents in the other phases have the same magnitude but are shifted in phase by 120^o (Das, 2007).

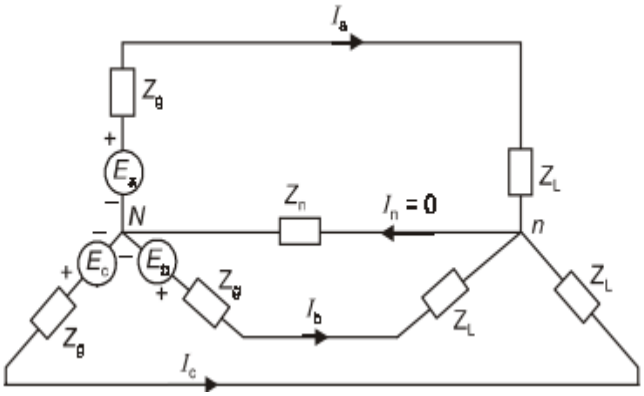


Figure 2.3: Balanced three phase network (Das, 2007).

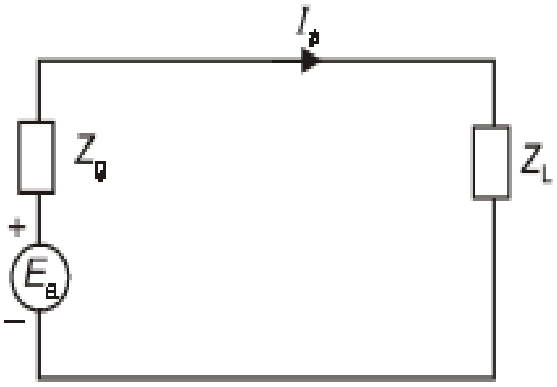


Figure 2.4: Single phase representation of a balanced three phase network (Das, 2007).

2.2.3.2 Transmission modelling problem

There are two general modelling for transmission problem, which are AC model and DC model. AC model is a complete and practical one, but it is complex. DC model is simple, but it contains simplification and approximations (Hemmati *et al.*, 2013). The advantages of AC model and disadvantages of the DC model can be concluded as follows:

a) DC model disadvantage

i. In DC modelling, the reactive power cannot be incorporated.

ii. The resulted plan for DC model should be reinforced when the AC operation is considered.

iii. Power losses is not considered in DC model

b) AC model advantage

i. Considers reactive power flow in the network.

ii. Power losses can be completely included.

iii. Reliability indexes can be calculated with the consideration of reactive power.

iv. Other types of studies such as voltage stability can be carried out (Hemmati *et al.*, 2013).

2.2.4 Bus Classification

In electrical power system analysis, four quantities are associated with each network bus. These are voltage magnitude |V|, phase angle ȝ, real power P and reactive power Q. In a power flow study, two out of four quantities are usually specified and the remaining two quantities are to be obtained through the solutions of equations as shown in Table 2.1. The system buses are generally classified into three categories (Das, 2007):

1. Slack Bus: Also known as swing bus and taken as reference where the magnitude and phase angle of the voltage are specified. This bus provides the additional real and reactive power to supply the transmission losses, since these are unknown until the final solution is obtained.
2. Load Bus: Also Known as PQ bus. At these buses, the real and reactive powers are usually specified. The magnitude and phase angle of the bus voltage are unknown until the final solution is obtained.
3. Voltage Controlled bus: Also known as the generator bus or regulated bus or P-|V| bus. At this bus, the real power and voltage magnitude are specified. The phase angle of the voltage

and the reactive power are unknown until the final solution is obtained. The limits on the value of reactive power are also specified.

Table 2.1: Bus Classification (Das, 2007).

Bus Type	Specified Quantity	Unknown Quantity
Slack Bus	|V|, ȣ	P, Q
Load Bus	P, Q	|V|, ȣ
Generator Bus	P, |V|	Q, ȣ

2.2.5 Power Flow Techniques

In Power System Engineering, the load flow study, also known as power flow study is an important tool involving numerical analysis applied to a power system, while solving the power flow problem assumption is taken as power system is a single phase model and is operating under balanced condition. Unlike traditional circuit analysis, a power flow study uses simplified notation such as a one line diagram and per unit (p.u) system, and focuses on various forms of AC power i.e. reactive, and real rather than voltage and current. It analyses the power systems in normal steady state operation and gives information about MW, MVar flows and bus voltages (Dharamjit, 2012).

Power flow analysis is performed to investigate the magnitude and phase angle of the voltage at each bus and the real and reactive power flows in the system components. The load flow results are very valuable for setting the proper protection devices to ensure the security of the system. The objective of any power flow program is to produce the following information (Onojo *et al.*, 2016):

i. Voltage magnitude at each bus.

ii. Real and reactive power flowing in each line.

iii. Phase angle of voltage at each bus.

iv. Power losses in each line.

There are three conventional method of power flow analysis, namely

a. Gauss-Seidel method
b. Newton Raphson method
c. Fast decoupled method

The Full Newton Raphson (NR) power flow is one of numerous power flow techniques (DC power flow, Backward Forward sweep, Gauss-Seidel) used for power system analysis. This method can readily be applied to strong and weakly mesh network, and has an advantage of accuracy, good convergence characteristics and low computation. The mathematical formulation of the Newton Raphson power flow techniques can simply be modeled as follows (Das, 2007):

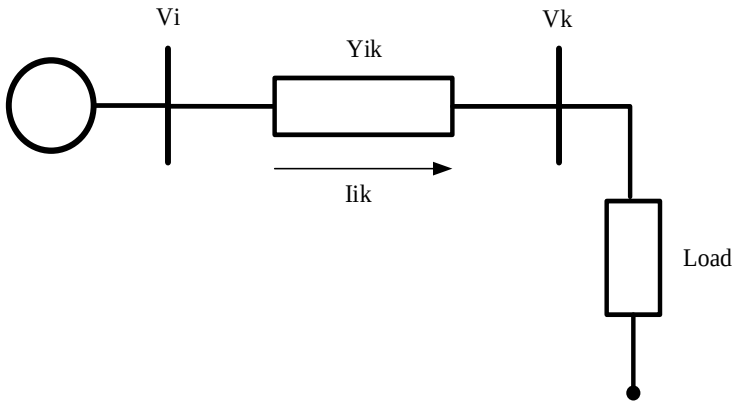


Figure 2.5: Single line model (Das, 2007)

From the Figure 2.5, consider bus i and k which are connected through element of admittance Y_{ik} in an n buses network having m voltage controlled buses (Das, 2007):

S = complex active power;

V = complex voltage;

I = complex current;

P = real power;

Q = reactive power;

δ = voltage angle;

θ = admittance angle;

P_{Loss} = real power loss;

Q_{Loss} = reactive power loss;

Y^o = shunt admittance/ grounding admittance;

$Y =$ transfer admittance

J_1 and J_4 are the decoupled jacobain square matrixes of size (n-1) and (n-1-m) respectively;

J_2 and J_3 are the coupled jacobain square matrixes of size (n x m) and (m x n) respectively;

Δq = change in parameter q;

$q^{(a)}$ = the value of parameter q at the ath iteration;

$|q|$ = absolute value of parameter q;

ik = from i to k;

$\varepsilon =$ Maximum absolute error

$$S = VI^* = P + jQ \tag{2.1}$$

$$S^* = V^* I = P - jQ \tag{2.2}$$

$$P_i = \sum_{k=1}^{n} |V_i|\,|V_k||Y_{ik}|\cos(\theta_{ik} - \delta_i + \delta_k) \tag{2.3}$$

$$Q_i = \sum_{k=1}^{n} |V_i|\,|V_k||Y_{ik}|\sin(\theta_{ik} - \delta_i + \delta_k) \tag{2.4}$$

$$P_{ik} = |V_i||V_k||Y_{ik}| \cos(\theta_{ik} - \delta_i + \delta_k) - |V_i|^2|Y_{ik}|\cos\theta_{ik} \quad (2.5)$$

$$Q_{ik} = -|V_i||V_k||Y_{ik}| \cos(\theta_{ik} - \delta_i + \delta_k) + |V_i|^2|Y_{ik}|\sin\theta_{ik} - |V_i|^2|Y_{ik}^o| \quad (2.6)$$

$$P_{Loss.ik} = P_{ik} + P_{ki} \quad (2.7)$$

$$Q_{Loss.ik} = Q_{ik} + Q_{ki} \quad (2.8)$$

$$I_i = \frac{P_i - jQ_i}{V_i^*} \quad (2.9)$$

Newton Raphson (NR) Method (Das, 2007):

$$\delta_i^{(a+1)} = \delta_i^{(a)} + \Delta\delta_i^{(a)} \quad (2.10)$$

$$|V_i|^{(a+1)} = |V_i|^{(a)} + \Delta|V_i|^{(a)} \quad (2.11)$$

$$\Delta P_i^{(a)} = P_i^{Scheduled} - P_i^{(a)} \quad (2.12)$$

$$\Delta Q_i^{(a)} = Q_i^{Scheduled} - Q_i^{(a)} \quad (2.13)$$

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} J_1 & J_2 \\ J_3 & J_4 \end{bmatrix} \begin{bmatrix} \Delta\delta \\ \Delta|V| \end{bmatrix} \quad (2.14)$$

Condition for termination of the iterations (Das, 2007):

$$max|V_i^{(a+1)} - V_i^{(a)}| \leq \varepsilon \quad (2.15)$$

$$\max |\Delta P| \leq \varepsilon \quad (2.16)$$

$$\max |\Delta Q| \leq \varepsilon \quad (2.17)$$

2.2.6 Contingency Analysis

A widely applied security assessment is contingency analysis. System analysis gives information about the oncoming event, and pertinent up-to-date information on the system conditions can be readily available to the system operator. This information is the outcome of offline system studies with real time network data (Dola & Chowdhury, 2006).

Contingency analysis is the study of the outage of elements such as transmission lines and generators, and investigation of the resulting effects on line power flows and bus voltages of the remaining system. It represents an important tool to study the effects of elements outage in power system security, during operation and planning. Contingencies referring to disturbances such as transmission element outages or generator outages may cause sudden and large changes in both the configuration and the state of the system. Contingencies may result in severe violations of the operating constraints. Consequently, planning for contingencies forms an important aspect of secure operation (Mohamed *et al.*, 2012). The results of contingency analysis give an idea about weak lines to ensure secure operation during contingencies which may result in severe violations of the operating constraints. Consequently, planning for contingencies forms an important aspect of secure operation. This analysis will present information on the happening of the system when a single element outage (N-1) occurs and predict the effect of outage on the network to ensure secure operation during contingencies (Wood & Wollenberg, 1996).

There are various methods of contingency analysis which include the following:

a) AC Load flow method

b) DC Load flow method

c) Performance Index method

Of all the above listed methods, AC power flow calculations are considered to be deterministic methods which are accurate compared to DC power flow methods. In deterministic methods, line outages are simulated by actual removal of lines (Nnonyelu *et al.*, 2014). The advantage of AC contingency analysis is that it provides the post-contingency power factor of the branch power flows besides detecting the bus voltage limit violations post contingencies (Mohamed *et al.*, 2012).

The most difficult methodological problem to cope with in contingency analysis is the accuracy of the method and the speed of solution of the model used. For accuracy, and when voltage is concerned, full AC load flow analysis is performed post each outage using the outage simulation to obtain post-outage line flows and bus voltages, and for each outage tested the contingency analysis procedure checks all power flows and voltage levels in the networks against their respective limits (Mohamed *et al.*, 2012). The use of AC power flow solution in contingency analysis is that it gives active, reactive power flows and magnitudes of bus voltage which will be used for the load shedding scheme (Abdulrazzaq, 2015). The Newton Raphson Power flow (NRPF), an algorithm under the AC load flow method is used to solve the power flow problems during the analysis using MATLAB. This is because the NRPF method has more accuracy than other AC Load flow methods and converges faster and also allow for gauging voltage/VAR effects (Manikandan & Bhoopathi, 2013; Nnonyelu *et al.*, 2014).

2.2.6.1 Line outage model

Transmission-line failures cause changes in the flows and voltages on the transmission equipment remaining connected to the system. Therefore, the analysis of transmission line failures requires methods to predict these flows and voltages so as to be sure they are within their respective limits (Soman *et al.*, 2015c). The transmission line outage is carried out by the formulation of the corresponding admittance matrix and the outages modelled by simply removing the line

information from the line data matrix (Mohamed *et al.*, 2012). Assume that the line connected between buses *m* and *n* will be the outage. The elements of the admittance [Y] matrix Equations (2.18 - 2.21) that will be affected are Ymm Ynn Ymn and Ynm and the new values of those admittances will be given by (Mohamed *et al.*, 2012):

$$Y^{'}mm = Ymm - \frac{1}{(Rmn + jXmn)} - \frac{jBmn}{2} \tag{2.18}$$

$$Y^{'}nn = Ynn - \frac{1}{(Rnm + jXnm)} - \frac{jBnm}{2} \tag{2.19}$$

$$Y^{'}mn = Ymn - \frac{1}{(Rmn + jXmn)} \tag{2.20}$$

$$Y^{'}nm = Ynm - \frac{1}{(Rnm + jXnm)} \tag{2.21}$$

Where:

$Y'mm, Ymm$: Self admittance at bus m post and pre-contingency.

$Y'nn, Ynn$: Self admittance at bus n post and pre-contingency.

$Y'mn = Y'nm$: Mutual admittance between bus m and n post-contingency

$Ymn = Ynm$: Mutual admittance between bus m and n pre-contingency

$jBmn, jBnm$: Shunt susceptance of the line.

2.2.6.2 Generating unit outage model

The generating unit outage model mainly consist of outage of one unit (or more) in a power station. Let the total generation for the station at bus (*i*) be P_{gi} (Mohamed *et al.*, 2012):

$$P^{'}_{gi} = P_{gi} - n\frac{P_{gi}}{g} \tag{2.22}$$

Where:

P'_{gi} : Active power generated at bus m post outage.

P_{gi} : Active power generated at bus m pre-outage.

n : Number of outage generation unit.

$\frac{P_{gi}}{g}$: Active power generated at bus m per a generator unit.

2.2.7 Contingency Ranking

Since contingency analysis process involves the prediction of the effect of individual contingency cases, the process becomes very tedious and time consuming when the power system network is large. In order to alleviate the above problem contingency screening or contingency selection process is used. Practically it is found that all the possible outages does not cause the overloads or under voltage in the other power system equipments. The process of identifying the contingencies that actually leads to the violation of the operational limits is known as contingency selection (Roy & Jain, 2013). One of the easiest ways to provide a quick calculation of possible overloads is by the linearization of nonlinear equation. These linear factors show the approximate change in line flows for changes in the network configuration (Soman *et al.,* 2015c). The choice of performance index to calculate depends on the engineer, physical properties of the system should be taken into consideration. The most common form of system performance indices give a measure of the deviation from rated values of system variables such as line flows, bus voltages and bus power injections. Contingencies are ranked in the order of their performance index values and processed starting with the most severe contingency at the top of the list proceeding down the ranking to the less severe ones. The performance indices are calculated for contingency cases with real flow violations and voltage violations (Mohamed *et al.,* 2012). The indices include Voltage Stability Index (VSI), Active Power Loading Performance Index (APLPI), Line Outage Distribution Factor

(LODF), Line loadability amongst others (Nnonyelu *et al.*, 2014). In this research work, APLPI will be adopted due to its ability to determine the active power loading on a particular line.

2.2.7.1 Active power loading performance index (APLPI)

Contingencies are ranked in the order of their performance index values and processed starting with the most severe contingency at the top of the list proceeding down the ranking to the less severe ones. The performance indices are calculated for contingency cases with real flow violations and voltage violations (Roy & Jain, 2013).

The APLPI is the active power loading performance index corresponding to line real power flow violations calculated using the conventional power flow algorithms for individual contingencies in an offline mode. It is formulated by APLPI Equation (2.23) and gives measure of line MW overloads (Mohamed *et al.*, 2012):

$$APLPI = \sum_{i=1}^{NL} W_{pi} \left(\frac{P_{ipc}}{P_{iLim}} \right)^{2m} \tag{2.23}$$

Where:

P_{ipc} : The post-contingency active power on line *i*

P_{iLim} : The active power flow limit on line *i*

$W_{pi} = 1/2m$: The weight factor of active power flow on line *i*

NL : Number of transmission lines.

m : is a positive integer ranging (1-30)

The post contingency line flows and bus voltages are obtained from the load flow solution after the application of the outage. The exponent (m) of the performance index is changed in the range from 1 to 30 to avoid masking errors, if (m) is a large number, the index will be a small number if

all flows are within limits, and it will be large if one or more lines are overloaded. Outages are then ranked on the basis of their corresponding performance indices. In this study the contingencies are ranked on the basis of line loading (Mohamed *et al.*, 2012; Roy & Jain, 2013).

2.2.8 Forced Islanding Scheme

As often seen sometimes, during a disturbance, the system tends to break up into islands. This occurs on account of the tripping measures adopted by the grid's protective systems. Undervoltages created in such situations aggravate the existing condition and lead to individual island failures. Unintentional or natural islanding has the potential to damage equipment and compromise system security (Dola & Chowdhury, 2006).

Forced islands are islands which are already predefined from offline studies which when emergency conditions occur, it selects appropriate breakers to open in order to prevent threshold violations and subsequent cascade failure, this occurs on account of tripping measures adopted by the grid's protective system. Forced islands (controlled island) is one of the last resort to prevent a widespread blackout in the power system under severe disturbance. The main purpose of controlled islanding is to split the original interconnected power network into several independent islands by disconnecting properly selected transmission lines (Song *et al.*, 2014). For implementation of the forced islanding scheme, islands for each outage case are already predefined, the predefined islands are selected in such a way that load demand approximately equals generation in the islands. After splitting the system into islands, load flow analysis is carried out on each island and power mismatch is calculated in each island to check the tolerance limit of voltage ±10%V to prevent the individual islands from collapse (Soman *et al.*, 2015a). In modern interconnected power systems, the reactive power can be locally compensated for, so the balance of active power is the most important requirement for the correct operation of power systems.

Power imbalance between generation and load can affect the stability of power systems. Therefore, one important requirement for an islanding strategy is to minimize the imbalance of active power within each island to facilitate minimum load shedding and system restoration (Song *et al.*, 2014).

The conditions used for determination of these islands are (Dola & Chowdhury, 2006):

i. Generation to load balance

ii. System bus voltage should remain within limits

iii. Line flows must not exceed loading limits.

iv. The number of loads shed should be as minimum as possible.

Any violation of the listed conditions, load shedding is then considered. Controlled islands are more stable than the unintentionally formed islands, and are also less prone to collapse and do not aggravate existing conditions that lead to blackouts (Zhenzhi *et al.*, 2016).

2.2.9 Load Shedding Scheme

A load shedding scheme usually composed of several stages and each stage is characterized by frequency/voltage threshold, amount of load, and delay before tripping.The number of Load shedding steps, amount of load that should be shed in each step, the delay between the stages, and the location of shed load are the important objects that should be determined in a load shedding algorithm. The objective of an effective load shedding scheme is to curtail a minimum amount of load, and provide a quick, smooth, and safe transition of the system from an emergency situation to a normal equilibrium state (Bevrani *et al.*, 2010). Once the threshold deviation is so large that the event is cosidered to be a large disturbance, all selected loads will be shed in one step without any intentional delay, it speeds up the necessary load shedding operation and prevents probable system instability due to delays (Seyedi & Sanaye-Pasand, 2009).

Nowadays, power system networks mostly operate closer to their stability limits as a consequence of the deregulated electricity market and growth in energy consumption. Under such operating conditions, a severe disturbance such as a loss of generating units or faults along transmission lines may lead to cascading events. Thus, the risk of collapse of the overall power system is increased (Tang et al., 2013). The formation of autonomous island which is of interest is only possible with a condition that there is sufficient generation to meet the local loads, otherwise load shedding can be taken to stabilize the grid (Mohamad *et al.*, 2011). The technical issues in achieving safe and smooth operation of islanded events are speed governor response, range of operating power, voltage and frequency control, earthen or equivalent protection of the island operation. Among these technical issues, voltage and frequency control tends to occur more frequently, of which load shedding is considered the most effective technique to overcome the problem. The most common factors contributing to power blackouts is the voltage instability issue arising from the overloading of the transmission system, which may result in a cascading or islanding event leading to blackout (Laghari *et al.*, 2013). The only means of stabilizing the voltage and frequency to their nominal values in an islanded system is by rejecting several loads through a load shedding scheme (Khamis *et al.*, 2015). The distributed power fluctuations negatively contributes to the power imbalance, frequency and voltage deviations. Significant disturbance can cause under/over frequency/voltage relaying and disconnect some lines, loads and generations. Under unfavorable conditions, this may result in a cascading failure and system collapse (Bevrani *et al.*, 2010).

Typically, the load shedding protects against excessive frequency or voltage decline by attempting to balance real and reactive power supply and demand in the system. Most common LS schemes are the Under Frequency Load Shedding (UFLS) schemes, which involve shedding predetermined amounts of load in the affected area if the frequency drops below specified frequency thresholds

to prevent the complete collapse of the island, such action must be taken promptly and must be sufficient to enable the remainder of the system to recover from the under frequency condition. The Under Voltage Load Shedding (UVLS) schemes, in a similar manner, are used to protect against excessive voltage decline (Bevrani *et al.*, 2010).

Conventional load shedding techniques are of two types (Laghari *et al.*, 2013):

i. Under frequency load shedding (UFLS)

ii. Under voltage load shedding (UVLS)

2.2.9.1 Under frequency load shedding

Under frequency load shedding (UFLS) is applied in the case of a severe fault, faster decrease in frequency due to the loss of generators. For this purpose, certain frequency threshold values are set to start the under frequency load shedding. The minimum acceptable frequency is dependent on the system equipment, such as the generator type, its auxiliary device, and the turbine. The UFLS relay is initialized to shed a fixed amount of load in predefined steps when frequency falls below a certain predefined threshold in order to prevent a blackout (Tang et al., 2013). In some cases events causing frequency to drop are followed by other events causing voltage drop. In these cases, since loads are voltage dependent, total system load is reduced and system frequency might not decrease so much to activate UFLS relays. However, the system could eventually collapse due to voltage instability (Seyedi & Sanaye-Pasand, 2009).

2.2.9.2 Under voltage load shedding

Under Voltage Load Shedding (UVLS) techniques are implemented to protect the power system from voltage collapse. Voltage instability generally occurs due to either forced outage of the generator or the line, or overloading. When this happens, the active and reactive power demand in

transmission lines varies severely and may cause a blackout if not recovered quickly. The UVLS technique is applied by power utilities to prevent voltage instability and restore voltage to its nominal value (Laghari et al., 2013). Reduction of load's active power consequently alleviates the load-generation imbalance, which causes relative recovery of bus voltages and thereafter load's active power brings the load-generation imbalance back to its real situation (Hoseinzadeh *et al.*, 2016). Under voltage load shedding can be a low cost alternative to constructing new transmission lines or new generation to maintain system security.

The load shedding scheme is a function of each load to be shed at each bus, based on the voltage level in the busbar and power flow in lines. The purpose is to determine the optimal quantities of active power to shed (López et al., 2016). The flow chart of conventional load shedding techniqueis shown in Figure 2.6.

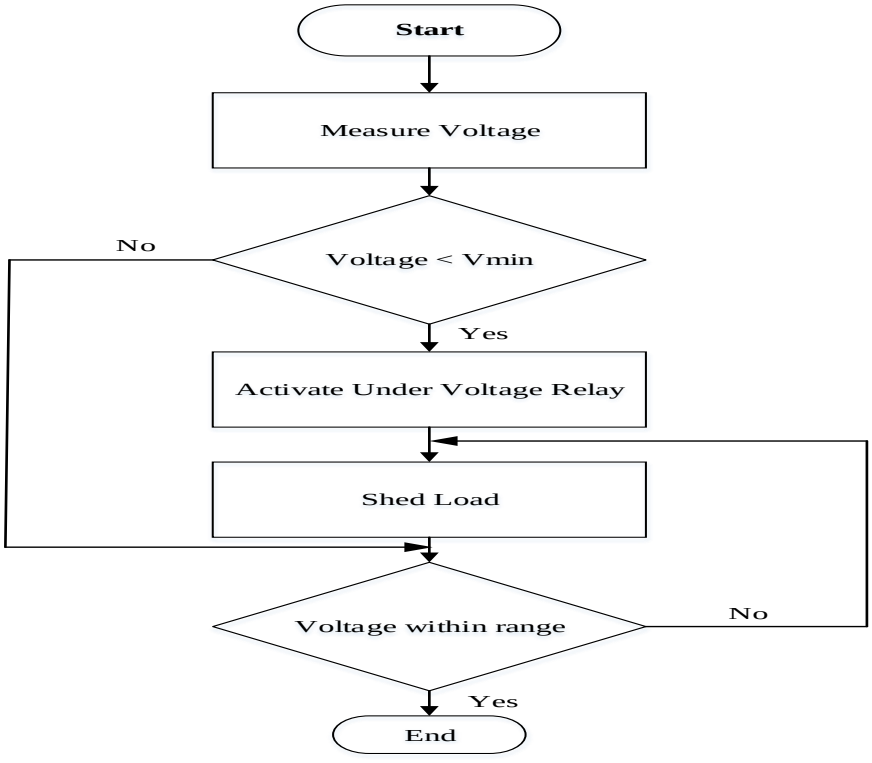


Figure 2.6: Conventional load shedding technique flow chart (Larik & Mustafa, 2016)

2.2.10 Objective Function for the minimization of load shed

Bus voltage level has a straight forward relation to buses with considerable changes in its operational state after a disturbance. The Under Voltage Load Shedding (UVLS) scheme is formulated such as to minimize the total load shed by considering operational and stability constraints. The objective function is defined as minimization of total real power to be shed, given by equation (2.24) Mageshvaran and Jayabarathi (2015).

$$J = min \sum_{i \in NLS} LS_i \tag{2.24}$$

Where NLS is set of buses selected for load shedding,

LS_i is amount of real power load shed at bus i.

This function is subject to the following inequality constraints;

(i) $$0 \le LS_i \le LS_{i\max} \qquad i \le NLS \tag{2.25}$$

Where LS_i is amount of real power load shed and

$LS_{i\max}$ is the maximum permissible load shed at i^{th} bus.

Actually, the permissible load shed is a fraction of total load at each selected bus. It may be considered the permissible amount of load shed is 90% of the total load at that bus and the remaining 10% of the total load may be required during emergency condition Mageshvaran and Jayabarathi (2015).

(ii) After load shed voltage of all load buses should be within the limit.

$$V_{i\min} \le V_i \le V_{i\max} \tag{2.26}$$

Where V_i is voltage magnitude at bus i, $V_{i\min}, V_{i\max}$ minimum and maximum bus voltage magnitude

After the contingency, if the voltage is below 0.945 pu, a corrective control schould be abel to get the voltage up to 0.945 pu or higher (Mageshvaran & Jayabarathi, 2015).

(iii) Maximum line flow constraints

$$L_{fi} \leq L_{f\max} \tag{2.27}$$

Where L_{fi} line flow in bus i, and $L_{f\max}$ is maximum permissible line flow on bus i.

The load shedding algorithm is also formulated in terms of both active and reactive power equality constraints (P and Q) given by (López *et al.*, 2016):

$$P_{Gi}^{0} - P_{Di}^{0} + \Delta P_{Di} = \sum_{j=1}^{N} |V_i||V_j||Y_{ij}|\cos\left(\delta_{ij} + \delta_j - \delta_i\right) \tag{2.28}$$

$$Q_{Gi}^{0} - Q_{Di}^{0} + \Delta Q_{Di} = -\sum_{j=1}^{N} |V_i||V_j||Y_{ij}|\sin\left(\delta_{ij} + \delta_j - \delta_i\right) \tag{2.29}$$

For a reliable operation, the constraints must be satisfied, after the defense scheme has returned the system from an emergency condition that could lead to cascade failure to an operating state, are (Dola & Chowdhury, 2006):

i. System bus voltage should remain within limits.

ii. Line flows must not exceed the line's maximum loading limit.

iii. Number of loads shed should be minimum.

2.2.11 Standard IEEE test systems

The IEEE test systems are standard test benchmarks designed by Institute of Electrical and Electronics Engineers (IEEE) for researchers to have a common testing platform and for easier

comparison. Few among the standard distribution testing benchmarks include: IEEE 6-bus test system and IEEE 14-bus test system with 100MVA base.

2.2.11.1 The standard IEEE 6-bus system

This is a standard transmission test system represented by a single line diagram as shown in Figure 2.7. The 6 bus test system consists of buses 2 and 3 as generator with bus 1 as the slack bus, three load buses 4, 5 and 6, with eleven interconnecting lines. The information for its bus data and line data is given in Appendix A (Soman *et al.*, 2015d).

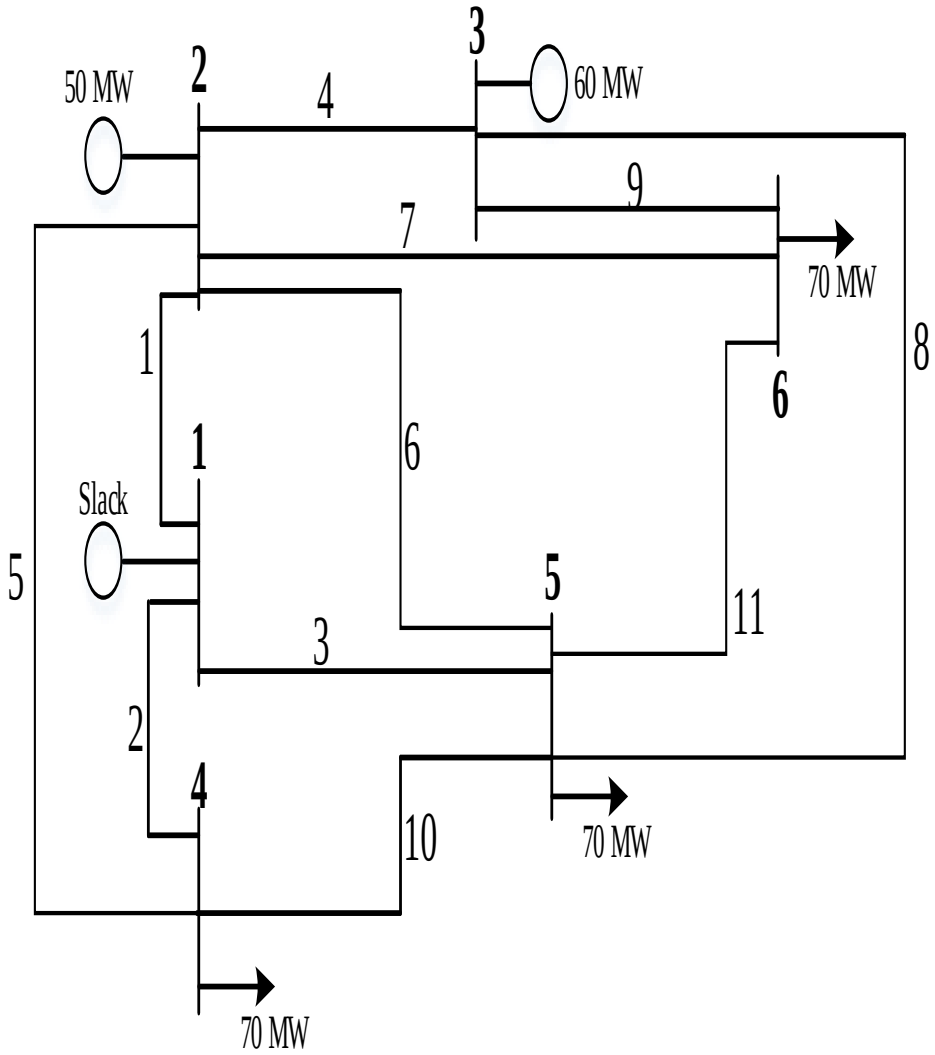


Figure 2.7: Single Line Diagram of IEEE 6 Bus test System (Soman *et al.*, 2015b).

2.2.11.2 The standard IEEE 14-bus system

This test system as represented by a single line diagram consist of 14-buses, 5 generator buses, 11 load buses with load totalling 259 MW, and 20 interconnecting lines, the single line diagram is as shown in Figure 2.8. The information for its bus and line data is given in Appendix B

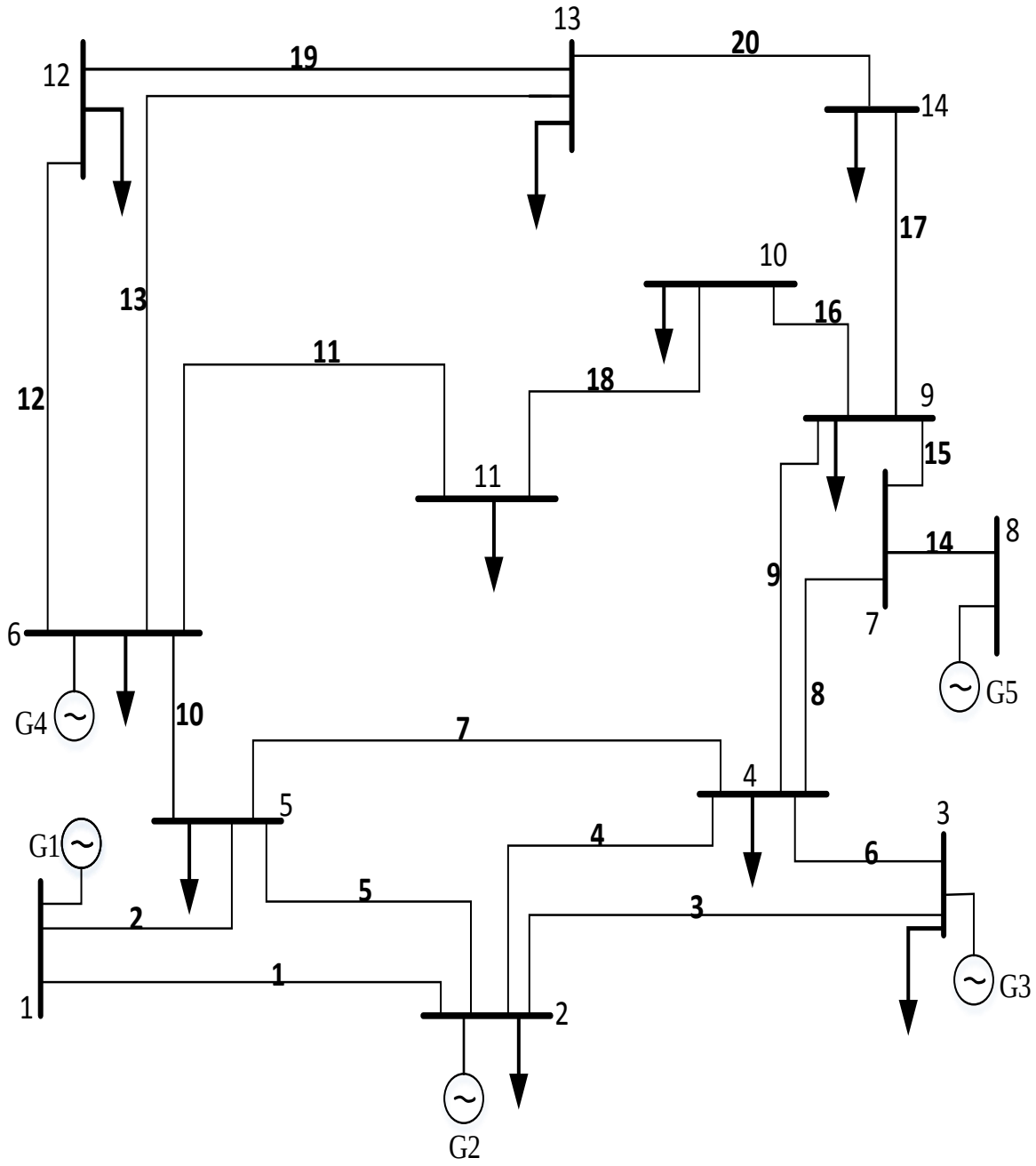


Figure 2.8: Single line diagram of IEEE 14-bus test system (Ketabi & Fini, 2015)

2.3 Review of Similar Works

The review of similar work gives an overview of the methods and approaches that have been used by other researches in the area of contingency analysis, island formation and load shedding scheme. They are presented as follows:

Dola and Chowdhury (2006) proposed a blackout mitigation technique which is based on strategic tripping of overloads, lines near the initial failure, and a load shedding strategy to curtail excess load to reestablish the normal operating conditions. The methodology consist of exploring the use of predetermined islanding scenarios along with load shedding scheme, in the work contingency analysis was carried out for its security assessment, and a load shedding is carried out before the islanding with distributed generation placement considered at some buses. The drawback of this strategy is the dependence of the islands formed on the geographical aspects of the grid, the suggestion to install new generation at selected buses which might not be optimally placed and capital intensive, and also islands formed after the load shedding does not guarantee a balance of load and generation, and will require loads to be dropped again after the islanding in order to obtain a stable system.

Wang *et al.* (2010) developed a novel method for the splitting boundary of power system controlled islanding, the aim of which is to minimize the load-generation imbalance in each island by considering the bus combination with lowest imbalance as the best option. The method contains three phases, namely, defining the domain of each generator according to power flow tracing algorithm, determining an initial splitting boundary based on the grouping information of generators after a system fault, and refining to get the final splitting boundary. However the choice of load flow method, which is power flow tracing should be done separately for both active and

reactive power, as the direction of the reactive power flow from a generator through a particular line may not be same as the direction of the active power flow.

Mohamed *et al.* (2012) analyzed power system contingency to detect network weakness and overloaded lines that may lead to cascade outage and complete blackout of the Sudan National grid. The work outlines mathematical models for the simulation of transmission line outage and generator outage. A full AC power flow contingency analysis routine was used for maximum accuracy and to provide the post-outage power factor of the branch power flows. For its contingency ranking Active Power Loading Performance Index is used to rank the element outage based on severity. However, the work only states the network weakness and suggest transmission and other elements capacity increment which is capital intensive.

Lin *et al.* (2014) developed a new controlled islanding methods based on power flow tracing for identifyng different islanding scheme for the fault at all buses. The power flow tracing method uses proportional sharing principle to show the contribution between nodes, and weakly connected nodes are considered as boundary nodes for island zone formation. The New England 10-generator 39-bus power system was used to demonstrate the proposed scheme. This method requires circuit breakers at almost every node in the network, as the island zone is dependent on the particular location of fault, and also power flow tracing methods does not distinguish between the generators with the same power output, while their reactive power productions are different.

Nnonyelu *et al.* (2014) performed reliability evaluation and contingency analysis of the Nigerian power system to determine the security level of the system. The contingency analysis made use of Newton-Raphson load flow method which is an AC power flow method because of its higher accuracy although computationally extensive when compared to DC power flow method. Also, the contingency analysis was ranked based on System Line Overload Index (SLOI). This research

work presented two important contingency event which are line outage and generator outage, but considered only the line outage in its contingency analysis and reliability evaluation overlooking the effects of generator outage which is important as a single generator outage affects the entire power redistribution, this limits the application of the findings in this research work on the 330KV Nigerian transmission system.

Li *et al.* (2014) proposed a zone division scheme based on power system sensitivity analysis of the power system, here the power system is divided into small potential areas for efficient power system operation and control. In the work buses and branches are lump up and regarded as one bus after N-1 contingency analysis, potential areas which satisfy N-1 contingency criterion was considered as one zone and those tie lines which do not satisfy N-1 contingency are regarded as zone boundaries. Only the tie line contingency analysis is considered, decreasing the computation amount of the N-1 contingency analysis. But lumping up the buses leads to approximation and does not reflect the true system characteristics, also the conditions that satisfy the N-1 contingency is not evident.

Soman *et al.* (2015a) developed a forced islanding and load shedding scheme, the aim of the work is to develop an algorithm to safely island, and load shed a 6-bus network in order to avoid cascade failure and total blackout. The algorithm developed identifies the risk during an outage as it occurs, and splits the system into predefined islands, the scheme use DC load flow studies and sensitivity factors to calculate overloads caused by the outage and an under voltage load shedding is used to stabilize islands found to be unstable. The scheme uses DC load flow analysis whose approximation is a major drawback and does not account for line losses, also the stages involved in the load shedding process sheds load at constant value of 1 MW after every iteration, which is computationally intensive and takes time before the stability is attained.

Soman *et al.* (2015b) Predetermined forced islanding and load shedding scheme was developed, and applied once a prospective cascading outage initiating event is predicted using contingency analysis which is a widely adopted security analysis method. This work is similar to the previous work of the authors (Soman *et al.*, 2015a). To detect the state of the system, continuous DC load flow analysis was used, Generation Shift Factors and Line Outage Distribution Factors is used as the linear sensitivity factors to show the level of line overloads. IEEE 6-bus system was taken as the case study, and all analysis carried out in MATLAB environment. However, the scheme uses DC load flow analysis whose approximation is a major drawback and does not account for line losses, and also the stages involved in the load shedding process drops excess load at 1 MW after every iteration, this takes time before the stability of the islanded system is reached.

Khamis *et al.* (2015) presented a new islanding detection and load shedding scheme developed based on the phase-space technique and using a probabilistic neural network-based classifier. The load shedding scheme is developed based on the backtracking search algorithm and comes in after the system detects unintentional islanding to prevent system collapse. The effectiveness of the scheme was tested on IEEE 33-bus radial system using MATLAB software environment. The limit of this scheme is that it's only applicable to radial Networks, and also the work recommended four islands on the 33-bus network, which can lead to unstable zone by reintroducing disturbances into the power system, and cause resynchronization issue when connecting back to the grid.

López *et al.* (2016) proposed a methodology for under voltage load shedding using a metaheuristic optimization technique (Particle Swarm Optimization) and a stability criterion with the objective function of optimizing the voltage stability criterion to guide the evolution process. Classical criterion for the under voltage load shedding and a simplified voltage stability index which identifies critical buses in the system was considered in the research and tested on IEEE 14-bus

system. But the contingency analysis used is not documented and well stated, as the load shedding scheme is fully dependent on this information provided by the N-x contingency analysis.

In conclusion, based on reviewed literature, various methods have been proposed for the mitigation of blackout caused by contingencies. Most schemes consider either islanding or load shedding alone as the last defense to prevent total system collapse, which is not suffient enough. Some research considered both islanding and load shedding strategy, but used a highly approximated power flow thechnique for its analysis and without considering line losses which are present in all networks, also the load shedding process considers load drop of exactly 1 MW per iteration. This approach is time consuming. In this research work, an exact system representation is considered by using Newton Raphson technique for the power flow analysis, and a load shedding scheme is proposed as an improvement.

CHAPTER THREE

MATERIALS AND METHODS

3.1 Introduction

In this chapter, the materials and methods employed for the successful completion of this research are discussed.

3.2 Materials

The materials used for this research work and validation are as follows:

3.2.1 Simulation Environment

All simulations analysis was done using MATLAB R2013a, and carried out using HP-14r002ne with the following specification:

a) Processor: Intel(R) Core(TM) i5-4210u CPU @ 1.7GHz 2.40GHz.

b) Installed Memory (RAM): 8.00GB.

c) System type: 64-bit Operating system, x64-based processor.

Details of the program developed are provided in appendix D.

The computer specification is provided, as speed is considered as a performance matric in this research.

3.2.2 Transmission System Parameters

The standard IEEE 6 bus test system gotten from (Wood & Wollenberg, 1996) is adopted in order to evaluate the developed scheme, and also serve as a basis for comparison with the work of (Soman *et al.*, 2015a). All line data and bus data are provided in appendix A.

To show the performance of the developed scheme, a standard IEEE 14 bus network with information gotten from (Ketabi & Fini, 2015) was used, the line data and bus data is given in appendix B.

3.3 Methodology

The methodology used in carrying out the research work are discussed as follows:

3.3.1 Power Flow Analysis

For the test networks used in this work we perform Newton Raphson power flow analysis using the steps as listed to obtain the network parameters, with the flowchart shown on Figure 3.1:

i. Read the network parameters

ii. Form Ybus matrix and classify the buses into slack bus, generator bus and load bus.

iii. Assume missing variables unless it is specified. For the load buses $|V_i| = 1.0$ and $\delta_i = 0.0$. For voltage regulated buses $\delta_i = 0.0$

iv. Compute active and reactive power for each load bus from equations (2.3), and (2.4).

v. Compute the scheduled errors using equation (2.12) and (2.13) for each load bus.

vi. Compute the elements of the Jacobian Matrix to obtain the angle deviation and voltage deviation.

vii. Using the values obtained from (vi) modify the voltage magnitude and phase angle at all loads equations (2.11) and (2.12).

viii. Continue until scheduled errors active power and reactive power deviation are within error limits ($\in \leq 0.0001$).

ix. Calculate flows and power in all the lines equations (2.5) and (2.6).

x. Print the voltage magnitude, phase angle and total power loss

xi. Stop.

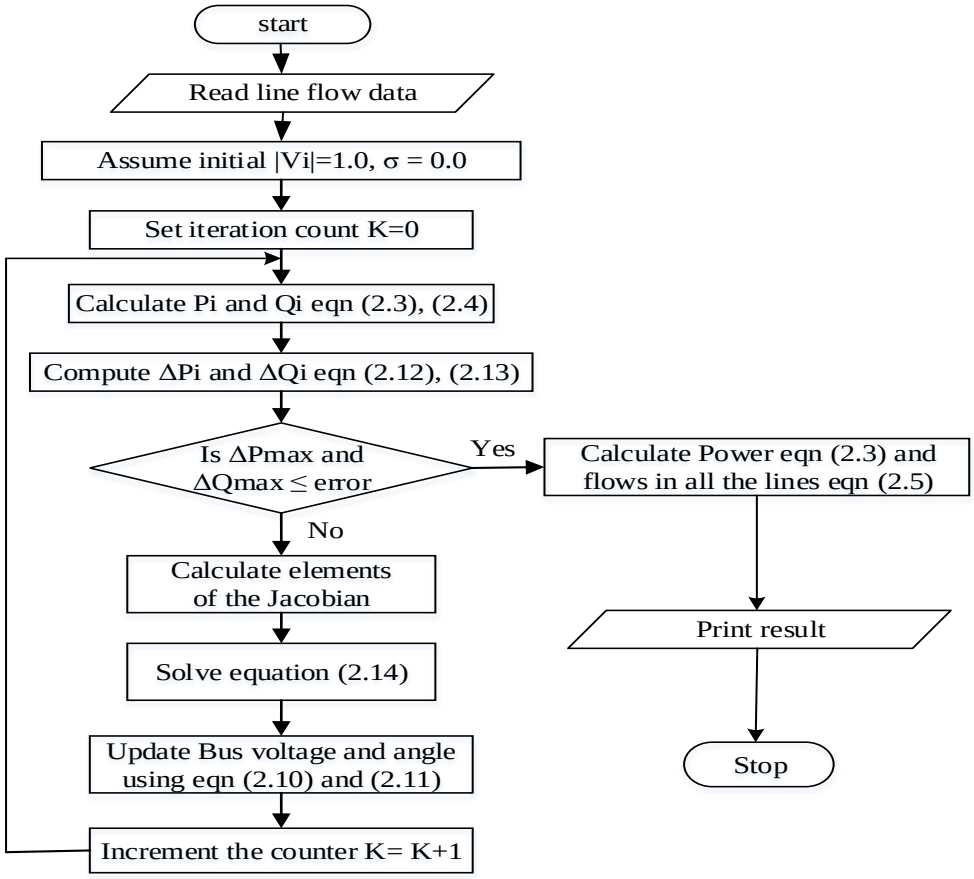


Figure 3.1: Flowchart for Newton Raphson technique (Das, 2007)

3.3.2 Contingency Analysis

For the contingncy analysis, an element (generator or line) is removed, to determine its effect in the network, in this research work, a single contingency (N-1) was considered. The flowchart is as shown in Figure (2.3), and the steps involved in carrying out the contingncy analysis are as follows:

i. Read the system bus data and line data

ii. Without considering the contingency, calculate base case power flow using Newton Raphson technique

iii. Simulate element outage by removing one line or generator from the network and proceed to the next step

iv. Using Newton Raphson Power Flow technique calculate the active power flow in the lines and voltage magnitude of each bus (post contingency power flow)

v. Calculate Active Power Loading Performance Index (APLPI) using equation (2.23), taking m= 1, W= 0.5

vi. Repeat (ii) to (v) until all N-1 contingencies are accounted for

vii. Rank the contingencies in descending order of the APLPI to obtain most severe cases

viii. Perform Newton Raphson Power Flow for the most severe contingency case

ix. Print the APLPI and Line Overloads

x. Stop.

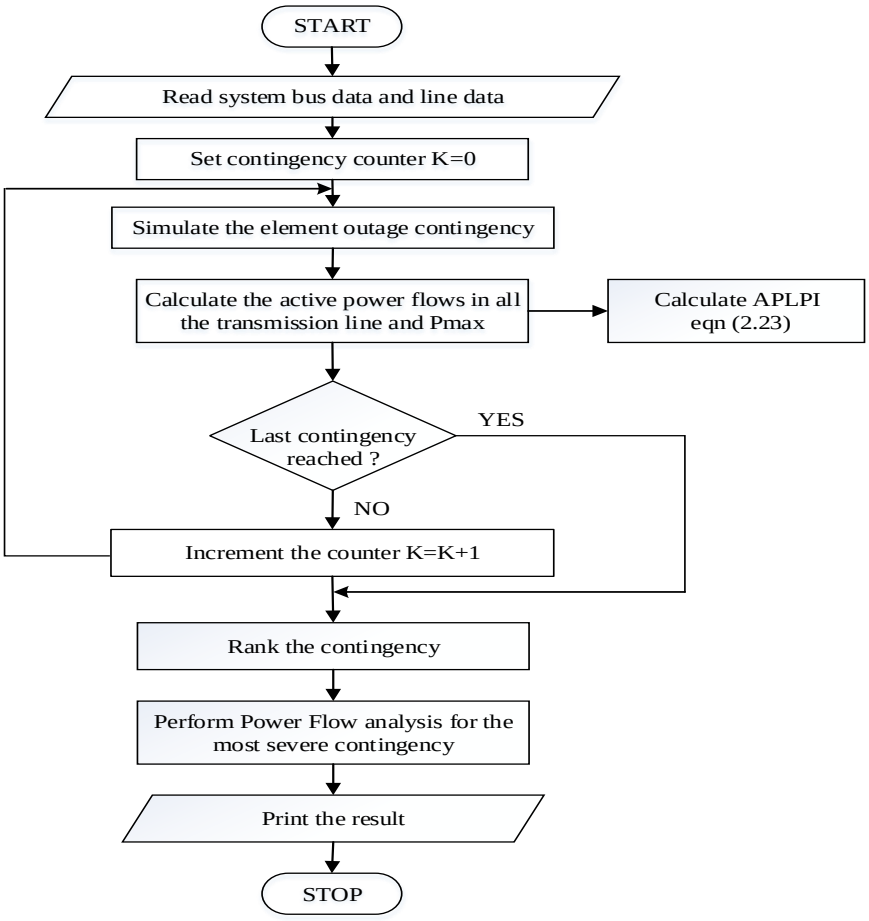


Figure 3.2: Contingency analysis flow using APLPI (Mohammed *et al.*, 2012)

3.3.3 Predefined Island

The Forced Island (predefined island) is formed using the system information by splitting of the network into two islands provided that a contingency causes violation, such that:

i. Both island contains generators buses and load buses.

ii. Most severe contingencies are split to different islands.

iii. Minimum power mismatch in the islands formed.

iv. Considering interconnecting branches for generation transfer to load.

The flowchart for the forced island is shown on Figure 3.3.

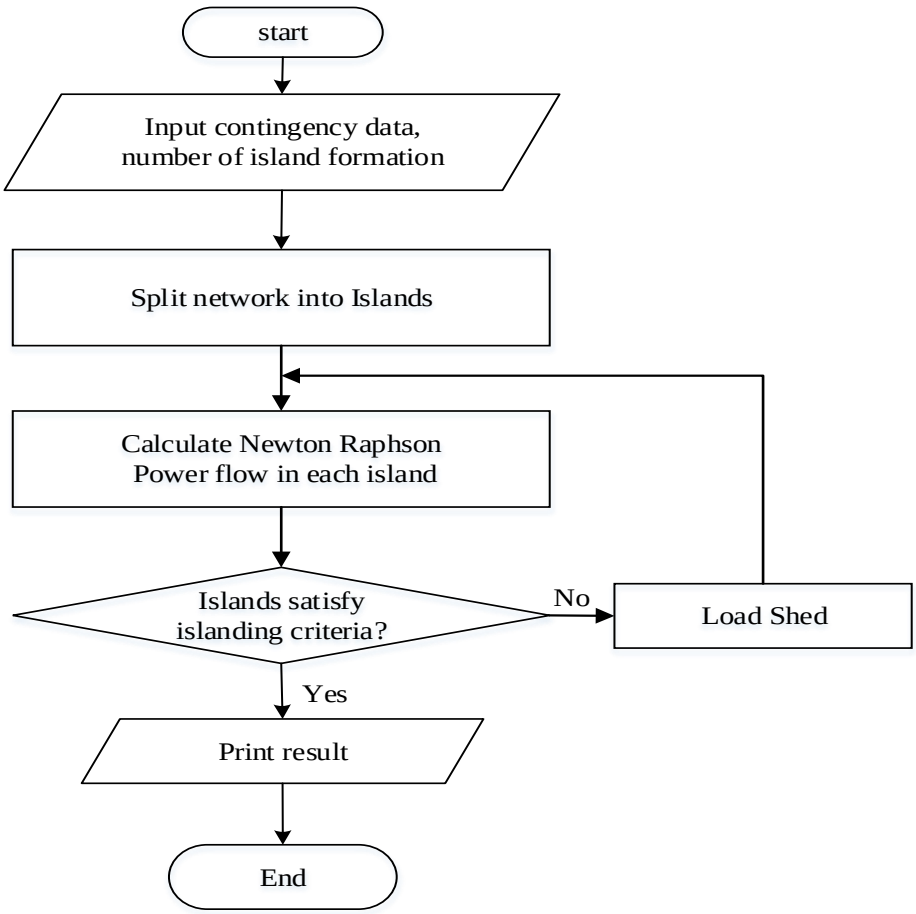


Figure 3.3: Flowchart for forced islanding scheme

3.3.4 Developing the load shedding scheme

i. Obtain the island load and generation data

ii. Run power flow to obtain the island new base case values of real power and voltage

iii. Calculate and check for maximum power mismatch ΔP

iv. If power mismatch, drop the load at the rate given by equation (3.1)

v. Run power flow to check for voltage violation as given by equation (2.26)

vi. Perform power flow to check line flow constraints given by equation (2.27)

vii. If voltage and line violation is present, select load on all PQ bus to shed

viii. For each step, repeat (v) to (viii) until no voltage bus and line limit violation

ix. Calculate total load shed and speed of load shedding.

For this research, to calculate the minimum load shed due to power imbalance, the power mismatch between the genetation and load in each island is added to the power loss in the network to serve as a tolerance limit .

Hence the minimum load shed is given by

$$\beta = \Delta P + \alpha \tag{3.1}$$

where $\beta =$ load to shed

ΔP Power mismatch

α = Tolerance limit,

The flowchart for the developed scheme is shown on Figure 3.4 which consist of the contingency analysis, predefined island, and load shedding scheme, all inclusive as one seamless algorithm.

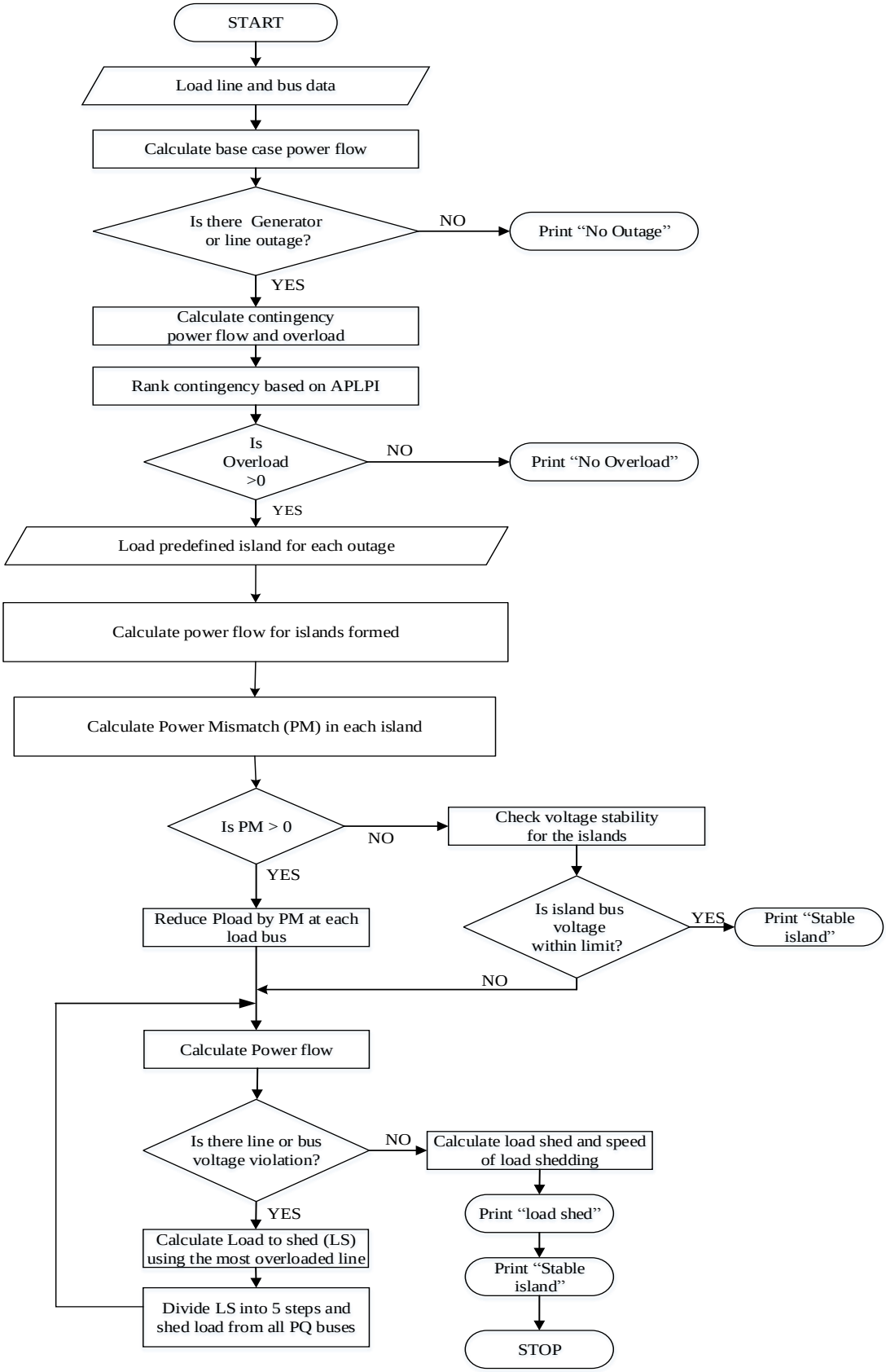


Figure 3.4: Flow chart of the developed contingency, island and load shedding scheme

3.4 Performance Evaluation

Voltage deviations and load shedding speed are the performance metrics used in this work when the load shedding is applied on the islands formed due to contingencies.

The bus voltage value should not deviate beyond $\pm 10\% V$ as explained in section 2.2.10. The value obtained from the voltage plots, and time graph of the developed method is compared to that of Soman *et al.,* (2015a).

To calculate the percentage improvement in load shed time and voltage magnitude, the equation (3.2) is used.

$$\text{Percentage Improvement (\%)} = \frac{|Y_a - Y_b|}{Y_a} \quad (3.2)$$

Where Y_a is the initial value, and Y_b is the final value.

CHAPTER FOUR

RESULTS AND DISCUSSIONS

4.1 Introduction

In this section, the performance of the method by Soman *et al.*, (2015a) and the developed method for optimal island and load shedding is discussed, and relevant results are reported, also the performance of the developed scheme is shown on IEEE 14 Bus system. All simulations are carried out on MATLAB R2013a software environment.

4.2 IEEE 6 Bus System

The IEEE 6 bus system as discussed in subsection (2.2.11.1) the bus and line data is given in appendix A. In carrying out the analysis on this bus, two case scenario are considered, the pre-contingency (base case), and the contingency.

4.2.1 Pre-contingency Analysis (Base Case)

For the pre-contingency, power flow was performed to determine the initial steady state of the network, and the power flow is performed using Newton Raphson power flow technique discussed in subsection (2.2.5), the procedure used in carrying out the precontingency analysis are given in subsection (3.3.1). The result obtained after performing the power flow in MATLAB are shown in Tables 4.1 and 4.2.

Table 4.1: Base Case Bus Data for 6 Bus system

Bus No	**V p.u**	**Angle degree**	**injection**		**Generation**		**Load**	
			MW	**MVar**	**MW**	**MVar**	**MW**	**MVar**
1	1.0500	0	108.0292	4.4596	108.0292	4.4596	0.00	0.00
2	1.0600	-3.8772	50.0	84.3690	50.0	84.3696	0.00	0.00
3	1.0800	-4.4482	60.0	90.3893	60.0	90.3893	0.00	0.00
4	0.9956	-4.2946	-70.0	-70.0	0.0	0.0	70.0	70.0
5	0.9948	-5.3697	-70.0	-70.0	0.0	0.0	70.0	70.0
6	1.0148	-6.0867	-70.0	-70.0	0.0	0.0	70.0	70.0
					218.0292	197.2179	210	210

From Table 4.1, bus 1 is a slack bus of 1.05 p.u. voltage magnitude, bus 2 and 3 are generator buses with real and reactive power supply of 50 MW and 60 MW respectively, and bus 4, 5, 6 are load buses. The total active power generation of 218.0292 MW and load of 210.00 MW, and a reactive power of 197.2179 MVar, and reactive load of 210 MVar was obtained for the precontingency analysis.

Table 4.2: Base Case line data for 6 bus system

From Bus	To Bus	P MW	Q MVar	From Bus	To Bus	P MW	Q MVar	Line Loss MW	Line Loss MVar
1	2	28.5133	-18.2329	2	1	-27.4743	20.3109	1.0390	2.0779
1	4	43.9035	19.0473	4	1	-42.8646	-14.8925	1.0387	4.1548
1	5	35.6125	11.3628	5	1	-34.5985	-7.5605	1.0140	3.8024
2	3	2.7614	-9.0095	3	2	-2.7219	9.2071	0.0395	0.1976
2	4	33.4631	51.5514	4	2	-31.7822	-48.1896	1.6809	3.3618
2	5	15.1899	18.1050	5	2	-14.6928	-16.6137	0.4971	1.4912
2	6	26.0600	15.2091	6	2	-25.4928	-13.5885	0.5672	1.6206
3	5	18.9700	26.7026	5	3	-17.8662	-24.3110	1.1038	2.3916
3	6	43.7519	62.0612	6	3	-42.7633	-57.1180	0.9887	4.9433
4	5	4.6470	0.0207	5	4	-4.6426	0.0664	0.0044	0.0871
5	6	1.8001	-7.2326	6	5	-1.7440	7.4010	0.0561	0.1684
Total								8.0292	24.2966

Table 4.2 shows the real power, reactive power and losses along the lines. The 11 interconnecting lines has a total real power loss of 8.0292 MW and a reactive power loss of 24.2966 MVar, the power loss was calculated using equation (2.7) and (2.8) respectively.

4.2.2 Contingency Analysis

For the contingency analysis, two case scenario were considered, the generator outage and the line outage.

4.2.2.1 Generator Outage Contingency analysis

The contingency analysis for the generator outage was performed based on the steps given in subsection (3.3.2). After the outage of the generator, power flow is performed as given in subsection (3.3.1) and the result obtained is shown in Table 4.3. The Active Power Loading Performance Index was calculated using equation (2.23) and the values obtained are ranked based on severity, from the most severe to the least severe.

Table 4.3: Generator contingency analysis result

Outage	Overloaded lines	APLPI	Overload (MW)	Combined Overload
Generator 2	1	1.7037	25.3770	
	2	0.7169	9.8715	
	3	0.6789	6.6093	41.8578
Generator 3	1	1.7861	26.7007	
	2	0.7810	12.4882	
	3	0.9643	15.5483	
	4	0.5859	1.6503	
	7	1.0335	13.1313	69.5188

From Table 4.3, it was observed that line 1, 2, and 3 are the most affected by the generator 2 outage with a total overload of 41.8578 MW. For the generator 3 outage, lines 1, 2, 3, 4, 7 were overloaded beyond their limit in Table A2, Appendix A with a total overload of 69.5188 MW. This implies that the outage of generator 2 will cause cascade failure of lines 1,2, and 3 which leads to system collapse. Also, the outage of generator 3 will cause cascade failure of lines 1, 2, 3, 4, and 7 leads to system collapse.

4.2.2.2 Line Outage Contingency analysis

The contingency analysis for the line outage was performed based on the steps given in subsection (3.3.2). After the outage of each line, power flow is performed and the Active Power Loading Performance Index (APLPI) are computed using equation (2.23). The numerical values obtained after performing the APLPI computation and power flow on MATLAB environment are shown in Table 4.4.

Table 4.4: Line contingency analysis result

Outage	Overloaded lines	APLPI	Overload (MW)	Combined Overload (MW)
Line 1	2	1.9456	10.9209	
	3	1.2429	7.5383	18.4592
Line 2	1	16.0592	30.3267	
	3	1.2929	13.7386	
	5	10.7901	29.2308	73.2961
Line 3	1	52.4994	19.8860	
	2	2.5276	11.8130	
	6	15.3376	7.3302	
	7	0.5675	4.1344	
	8	7.3122	6.2283	49.3919
Line 4	NIL	NIL	NIL	NIL
Line 5	2	10.1475	16.7754	
	6	0.5948	2.8157	
	8	1.3099	3.8386	
	7	0.1350	1.5174	24.9471
Line 6	8	0.9059	3.3552	
	7	0.1069	1.1102	
	3	0.0614	0.2224	4.6878
Line 7	3	0.0651	0.3531	
	6	0.3243	2.0597	
	9	0.0647	0.5126	2.9254
Line 8	6	0.0957	0.6138	0.6138
Line 9	1	0.2848	2.8516	
	7	2.6793	24.6140	
	8	29.7870	21.6221	
	11	0.0950	0.6054	49.6931
Line 10	NIL	NIL	NIL	NIL
Line 11	NIL	NIL	NIL	NIL

The contingency analysis for each of the line outage gives a combined overload of 18.4592 MW for line 1 outage, 73.2961 MW for line 2, 49.3919 MW for line 3, 24.9471 MW for line 5, for line 6 an overload of 4.6878 MW, for line 7 an overload of 2.9254 MW, 0.6138 MW for line 8, and for line 9 an overload of 49.6931 MW. The outage of lines 4, 10, 11 has no effect on the network, as the power flowing before contingency is redistributed after outage, without causing line limit violation. The values were obtained after performing the contingency and power flow analysis on MATLAB.

The overloaded lines caused by the outage of the individual generator and lines given by Tables 4.3 and 4.4 is summarized in Table 4.5.

Table 4.5: Summary of IEEE 6-bus contingency analysis

Outage case	**Overloaded line**
Generator 2	1, 2, 3
Generator 3	1, 2, 3, 4, 7
Line 1	2,3
Line 2	1, 3, 5
Line 3	1, 2, 6, 7, 8
Line 4	-
Line 5	2, 6, 7, 8
Line 6	3, 7, 8
Line 7	3, 6, 9
Line 8	6
Line 9	1, 7, 8, 11
Line 10	-
Line 11	-

4.2.3 Predefined Island 6 bus

The predefined islands are formed based on the information from the contingency analysis of generator outage and line outage, these predefined islands are selected in such a way that load demand is approximately equal to generation in the islands formed as discussed in sub-section (2.2.8). To prevent collapse of the entire system two islands are formed with respect to the specific outage that occurs, this is done to prevent cascade failure and reduce the total time to attain stable system after load shed. The steps used to determine the predefined islands is given in sub-section (3.3.3). Table 4.6 shows the predefined islands for each contingency case of the 6-bus network.

Table 4.6: Predefined island for each outage IEEE 6 bus

Outage Case	Island 1	Island 2
Generator 2	0,2,3,6	0,1,4,5
Generator 3	0,2,3,6	0,1,4,5
Line 1	1,2,4,5	0,0,3,6
Line 2	1,2,4,5	0,0,3,6
Line 3	1,2,4,5	0,0,3,6
Line 4	0,0,0,0	0,0,0,0
Line 5	0,2,3,6	0,1,4,5
Line 6	0,2,3,6	0,1,4,5
Line 7	0,3,6,0	1,2,4,5
Line 8	1,2,4,5	0,3,6,0
Line 9	0,1,4,0	2,3,5,6
Line 10	0,0,0,0	0,0,0,0
Line 11	0,0,0,0	0,0,0,0

From Table 4.6, outage of lines 4, 10 and 11 do not cause overload in the network and does not require safety measures for the outage. While outage of the generators and remaining lines require load shedding to prevent the islands from collapse.

4.2.3.1 Analysis of island One

In carrying out the analysis of island one, power flow was performed to obtain the initial (pre load-shedding) bus voltage, the overloaded lines, and also to determine the exact load required to be shed due to power mismatch, bus voltage violations and line limit violations.

The power mismatch is calculated to check the difference between the generation and load demand. For the case of power mismatch the load is shed as specified in subsection (3.3.4).

The generator and line pre load-shedding bus voltage magnitude, and post load-shedding bus voltage magnitude, overloaded lines and total load shed for island one, as analysed using power flow is presented in Table 4.7.

Table 4.7: Analysis of 6-bus island One

Outage	**Island bus**	**Pre load shed bus voltage (V)**	**Overloaded lines**	**Power mismatch**	**Load shed**	**Post load shed bus voltage (V)**
Generator 2	2	1.0500	-	10	16	1.0500
	3	1.0800				1.1200
	6	1.0077				1.0559
Generator 3	2	1.0500	-	20	25	1.0500
	3	1.0800				1.1200
	6	1.0077				1.0621
Line 1	1	1.0500	2, 3, 6	-	14	1.0500
	2	1.0600				1.0800
	4	0.9874				1.0069
	5	0.9404				0.9730
Line 2	1	1.0500	1, 3, 5, 6	-	64	1.0500
	2	1.0000				1.1000
	4	0.8839				1.0529

	5	0.8798				1.0122
Line 3	1	1.0500	1, 2, 6, 10	-	53	1.0500
	2	1.0000				1.0800
	4	0.9205				1.0168
	5	0.7737				0.9999
Line 4	-	-	-	-	-	-
Line 5	2	1.0500	-	-	-	-
	3	1.0800				-
	6	1.0077				-
Line 6	2	1.0500	-	-	-	-
	3	1.0800				-
	6	1.0077				-
Line 7	3	1.0700	9	10	16	1.0700
	6	0.9841				1.0057
Line 8	1	1.0500	5, 6	-	6	1.0500
	2	1.0600				1.0600
	4	0.9858				0.9937
	5	0.9403				0.9580
Line 9	1	1.0500	2	-	34.5	1.0500
	4	0.8365				0.9584
Line 10	-	-	-		-	-
Line 11	-	-	-		-	-

For island 1, the bus voltage for generator 2 and 3 outage remains within permissible limits after 16 MW and 25 MW load was shed respectively, this load is shed as a result of the load to generation difference in the island. For line 1 outage, lines 2, 3, 6 was overloaded, initial bus 5 voltage was 0.9404V which is out of range, but appreciated to 0.9730V after load shed of 14 MW in that island. For the line 2 outage, bus 4 and 5 voltage was 0.8839V and 0.8798V, and lines 1, 3, 5, 6 were

overloaded, the bus 4 and 5 voltage appreciated to 1.0529V and 1.0122V post load shed of 64 MW. For the outage of line 3, the island had a violation on lines 1, 2, 6, 10, on bus 5 with a voltage of 0.7737V, and bus 4 voltage 0.9205V but after load shed of 91 MW the bus voltage was restored to 0.9999V and 1.0168V respectively. Line 5 outage caused no line and bus voltage overload. Line 6 outage caused no overload on lines, and voltage violation was not recorded. For the outage on line 7, there was overload on line 9 which required load shed of 16 MW. Line 8 outage caused an overload on line 5 and 6, bus 5 voltage was recorded as 0.9403V, which appreciated to 0.9580V after a load shed of 16 MW. Line 9 outage caused an overload on the islands' line 2, and bus 4 voltage of 0.8365V, which required load shed of 34.5 MW to restore the voltage to 0.9584V.

4.2.3.2 Analysis of island Two

In carrying out the analysis of island two, power flow was performed to obtain the initial (pre load-shedding) bus voltage, the overloaded lines, and also to determine the exact load required to be shed due to power mismatch, bus voltage violations and line limit violations. The power mismatch is calculated to check the difference between the generation and load demand. For the case of power mismatch the load is shed as specified in subsection (3.3.4).

The generator and line pre load-shedding bus voltage magnitude, and post load-shedding bus voltage magnitude, overloaded lines and total load shed for island 2, as analysed using power flow is presented in Table 4.8.

Table 4.8: Analysis of 6-bus island Two

Outage	Island bus	Pre load shed bus voltage (V)	Overloaded lines	Power mismatch	Load shed	Post load shed bus voltage (V)
Generator 2	1	1.0500	2, 3	-	81.9	1.0500
	4	0.7957				0.9799
	5	0.7364				0.9632
Generator 3	1	1.0500	2, 3	-	91	1.0500
	4	0.7957				0.9949
	5	0.7364				0.9810
Line 1	3	1.0700	9	10	16	1.0700
	6	0.9841				1.0057
Line 2	3	1.0700	9	10	16	1.0700
	6	0.9841				1.0057
Line 3	3	1.0700	9	10	16	1.0700
	6	0.9841				1.0057
Line 4	-	-	-	-	-	-
Line 5	1	1.0500	2, 3		90.5	1.0500
	4	0.7957				0.9949
	5	0.7364				0.9810
Line 6	1	1.0500	2, 3		90.5	1.0500
	4	0.7957				0.9949
	5	0.7364				0.9810
Line 7	1	1.0500	5, 6		31	1.0500
	2	1.0600				1.0600
	4	0.9858				0.9902
	5	0.9403				0.9522
Line 8	3	1.0700	9	10	16	1.0700
	6	0.9840				1.0057

Line 9	2	1.0500	7, 8	30	84	1.0500
	3	1.1200				1.1200
	5	0.9779				1.0353
	6	0.9413				0.9960
Line 10	-	-	-	-	-	-
Line 11	-	-	-	-	-	-

Generator 2 outage caused an overload on lines 2 and 3, and voltage violation on bus 4 and 5, which required load shed of 81.9 MW to appreciate from 0.7957V to 0.9799V of bus 4 voltage, and 0.7364V to 0.9632V of bus 5 voltage. The outage of generator 3 caused violation of lines 2 and 3, with voltage violation on bus 4 and 5 which required 91 MW load drop to record 0.9949V from initial voltage of 0.7957V at bus 4, and voltage of 0.9810V from initial 0.7364V at bus 5. Line 9 was overloaded for the outage of lines 1, 2, 3 and 8 which required 16 MW load to be shed and also a volage appreciation from 0.9841V to 1.0057V. line 5 outage and line 6 outage caused a severe overload on lines 2, and line 3 which required a load shed of 90.5 MW for voltage at bus 4 to rise from 0.7957V to 0.9949V, and bus 5 voltage to rise from 0.7364V to 0.9810V. For the line 7 outage, line 5 and 6 was observed to be overloaded which required a load shed of 31 MW in that island, also bus 5 voltage appreciated from an initial 0.9403V to 0.9522V. Line 7 and 8 was observed to be overloaded from the outage of line 9, which required a load shedding of 84 MW for bus 6 voltage to reach 0.9960V from an initial voltage of 0.9413V.

From the analysis of island one, and island two. It is evident that the larger the deviation of the load bus voltage magnitude from the nominal value, the more the load required to be shed to have a stable system.

The average percentage improvement of the developed method and the method of Soman *et al.*, (2015a) over the base case voltage magnitude for all the outage is presented in Table 4.9. The percentage improvement was calculated using equation (3.2).

Table 4.9: Voltage Profile Improvement Over Base Case

Outage	**Voltage Improvement (%) Developed Method**	**Voltage Improvement (%) Soman et al (2015a)**
Generator 2	15.61	14.43
Generator 3	15.68	15.29
Line 1	2.13	1.89
Line 2	11.59	11.39
Line 3	13.99	11.77
Line 4	-	-
Line 5	29.13	26.27
Line 6	29.13	26.13
Line 7	1.30	0.92
Line 8	2.91	2.81
Line 9	8.75	8.52
Line 10	-	-
Line 11	-	-

An average voltage improvement of 13.02 % was achieved over the base case voltage for the developed method. For the method of Soman et al (2015a), an average voltage improvement of 11.94 % was gotten over the base case voltage. The bus voltage data used for the calculation of this improvement is contained in appendix C.

4.3 IEEE 14 bus System

The IEEE 14 bus system is discussed in subsection (2.2.11.2) the bus and line data is given in appendix B. In carrying out the analysis on this bus, two case scenario are considered, the pre-contingency (base case), and the contingency. The bus and line data for the standard 14 bus test system as given in appendix B was used in order to perform the contingency analysis, island formation and load shedding scheme, to show the performance of the developed method.

4.3.1 Pre-contingency Analysis (Base Case)

For the pre-contingency, power flow was performed to determine the initial steady state of the network, and the power flow is performed using Newton Raphson power flow technique discussed in subsection (2.2.5). The procedure used in carrying out the precontingency analysis are given in subsection (3.3.1). The result obtained after performing the power flow in MATLAB environment are shown in Table 4.10 and Table 4.11.

Table 4.10: Base case Bus Data for 14 bus system

Bus	V	Angle	Injection		Generation		Load	
No	pu	Degree	MW	MVar	MW	MVar	MW	MVar
1	1.0600	0	232.5929	-15.2331	232.5929	-15.2331	0.0000	0.0000
2	1.0450	-4.9891	18.3000	35.2276	40.000	47.9276	21.7000	12.7000
3	1.0100	-12.7492	-94.2000	8.7584	0	27.7584	94.2000	19.0000
4	1.0132	-10.2420	-47.8000	3.9000	0.0000	0.0000	47.8000	-3.9000
5	1.0166	-8.7601	-7.6000	-1.6000	0.0000	0.0000	7.6000	1.6000
6	1.0700	-14.4469	-11.2000	15.5261	0.0000	23.0261	11.2000	7.5000
7	1.0457	-13.2368	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
8	1.0800	-13.2367	0.0000	21.0303	0.0000	21.0303	0.0000	0.0000
9	1.0305	-14.8201	-29.5000	-16.6000	0.0000	0.0000	29.5000	16.6000
10	1.0299	-15.0360	-9.0000	-5.8000	0.0000	0.0000	9.0000	5.8000
11	1.0461	-14.8581	-3.5000	-1.8000	0.0000	0.0000	3.5000	1.8000
12	1.0533	-15.2973	-6.1000	-1.6000	0.0000	0.0000	6.1000	1.6000
13	1.0466	-15.3313	-13.5000	-5.8010	0.0000	0.0000	13.5000	5.8000
14	1.0193	-16.0717	-16.0717	-5.0000	0.0000	0.0000	14.9000	5.0000
Total					272.5929	104.5093	259.0000	73.5000

From Table 4.10, bus 1 is a slack bus of 1.06 p.u voltage magnitude, bus 2, 3, 8 and 10 consist of generators 2, 3, 4, and 5 respectively. The total active power generation is 272.5929 MW, and load of 259 MW, and a reactive power of 104.5093 MVar, and reactive load of 73.50 MVar was obtained for the precontingency analysis.

Table 4.11: Base case line data 14 bus network

From Bus	To Bus	P MW	Q MVar	From Bus	To Bus	P MW	Q MVar	Line Loss MW	Line Loss MVar
1	2	157.0804	-17.4841	2	1	-152.7718	30.6388	4.3086	13.1547
1	5	75.5126	7.9814	5	1	-72.7400	3.4641	2.7726	11.4455
2	3	73.3960	5.9362	3	2	-71.0628	3.8935	2.3332	9.8298
2	4	55.9430	2.9351	4	2	-54.2731	2.1320	1.6700	5.0670
2	5	41.7328	4.7376	5	2	-40.8128	-1.9287	0.9200	2.8089
3	4	-23.1372	7.7518	4	3	23.5284	-6.7535	0.3911	0.9983
4	5	-59.5849	11.5744	5	4	60.0640	-10.0631	0.4791	1.5113
4	7	27.0657	-15.3955	7	4	-27.0640	17.3272	0.0000	1.9317
4	9	15.4639	-2.6400	9	4	-15.4639	3.9320	0.0000	1.2920
5	6	45.8888	-20.8434	6	5	-45.8888	26.6170	0.0000	5.7736
6	11	8.2873	8.8976	11	6	-8.1646	-8.6407	0.1227	0.2568
6	12	8.0644	3.1760	12	6	-7.9837	-3.0081	0.0806	0.1678
6	13	18.3372	9.9811	13	6	-18.0853	-9.4852	0.2518	0.4960
7	8	0.0000	-20.3624	8	7	0.0000	21.0303	0.0000	0.6679
7	9	27.0657	14.7978	9	7	-27.0657	-13.8405	0.0000	0.9573
9	10	4.3928	-0.9044	10	9	-4.3868	0.9204	0.0060	0.0160
9	14	8.6368	0.3214	14	9	-8.5474	-0.1312	0.0894	0.1902
10	11	-4.6132	-6.7204	11	10	4.6646	6.8407	0.0514	0.1203
12	13	1.8837	1.4081	13	12	-1.8727	-1.3982	0.0110	0.0100
13	14	6.4580	5.0834	14	13	-6.3526	-4.8688	0.1054	0.2146
Total								13.5929	56.9096

Table 4.11 shows the real power, reactive power and losses along the lines. The 20 interconnecting lines has a total real power loss of 13.5929 MW and a reactive power loss of 56.9096 MVar, the power loss was calculated using equation (2.7) and (2.8) respectively.

4.3.2 Contingency Analysis

For the contingency analysis, the individual generator outage and line outage was considered. The contingency analysis was performed based on the steps given in subsection (3.3.2). After the outage of either generator or lines, power flow is performed and the Active Power Loading Performance Index is calculated for all the lines using equation (2.23) to obtain the overloaded lines. 24 outages cases was simulated by direct removal of a single line or generator to obtain the overloaded lines as given in Table 4.12.

Table 4.12: Summary of IEEE 14 bus Contingency Analysis

Outage Case	**Overloaded Line**
Generator 2	1, 2, 3, 7, 10
Generator 3	1, 2, 3, 7
Generator 4	1, 2, 3, 7
Generator 5	1, 2, 3, 7
Line 1	2, 3, 7, 10
Line 2	1, 3, 4, 5
Line 3	1, 2, 4, 5, 6, 7, 10
Line 4	1, 2, 3, 5, 7, 10
Line 5	1, 2, 3, 4
Line 6	1, 2, 3, 7
Line 7	1, 3, 4, 10
Line 8	1, 2, 3, 7, 10, 18
Line 9	1, 2, 3, 7, 10, 15
Line 10	1, 2, 3, 7, 8, 9, 11, 15, 16, 18
Line 11	1, 2, 3, 7
Line 12	1, 2, 3, 7, 10
Line 13	1, 2, 3, 7, 19
Line 14	-
Line 15	1, 2, 3, 7, 10, 18
Line 16	1, 2, 3, 7, 10
Line 17	1, 2, 3, 7, 10, 20
Line 18	1, 2, 3, 7
Line 19	1, 2, 3, 7, 10
Line 20	1, 2, 3, 7

From the Table 4.12, generator 2 outage caused the most overload on the lines (5 lines were overloaded). Line 10 outage causes the most line overloads (10 lines were overloaded), while line 14 outage caused no overload in the system.

4.3.3 Predefined Island

The predefined islands are formed based on the information from the contingency analysis of generator outage and line outage, these predefined islands are selected in such a way that load demand is approximately equal to generation in the islands formed as discussed in sub-section (2.2.8). To prevent collapse of the entire system two islands are formed with respect to the specific outage that occurs, this is done to prevent cascade failure and reduce the total time to attain stable system after load shed. The steps used to determine the predefined islands is given in sub-section (3.3.3). Table 4.13 shows the predefined islands for each contingency case of the 14-bus network.

Table 4.13: Predefined island for generator and line outage IEEE 14 bus

Outage	**Island 1**	**Island 2**
Generator 2	1, 2, 3, 4, 5, 6, 7 8,9,10,11,12,13,14	-
Generator 3	2, 3	1,4,5,6,7,8,9,10,11,12,13,14
Generator 4	2, 3	1,4,5,6,7,8,9,10,11,12,13,14
Generator 5	2, 3	1,4,5,6,7,8,9,10,11,12,13,14
Line 2	-	1, 2, 3, 4, 5, 6, 7 8,9,10,11,12,13,14
Line 3	2, 3, 4	1,5,6,7,8,9,10,11,12,13,14
Line 14	-	-
Line 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 17, 18, 19, 20	2, 3	1,4,5,6,7,8,9, 10,11,12,13,14

The bus selection for the predefined island one and island two for all line and generator outage is shown on Table 4.13. For the generator 2 outage and line 2 outage, no island is formed due to the nature of the network and the criteria listed in section (2.2.8), the outage of generators 3, 4, 5 forms island 1 containing bus 2, 3 while the other buses are contained in island 2. The outage of line 14 caused no overload, and does not require further protective action.

The active power overload as calculated from the power flow, and the total load shed as calculated considering the objective function equation (2.24), using the steps given in subsection (3.3.4) for the individual outage in both islands is presented in Table 4.14.

Table 4.14: Overload and load shed summary of IEEE 14 bus island One and island Two

Outage	**Island 1**		**Island 2**	
	Overload (MW)	**Load Shed (MW)**	**Overload (MW)**	**Load Shed (MW)**
Generator 2	147.19	114.3	-	-
Generator 3	62.37	78.90	12.7958	14.4000
Generator 4	62.37	78.90	8.2765	9.9000
Generator 5	62.37	78.90	8.2765	8.2765
Line 1	62.37	79.90	139.48	81.60
Line 2	-	-	218.39	180.30
Line 3	128.52	127.70	136.91	64.30
Line 4	62.37	79.90	139.48	83.60
Line 5	62.37	79.90	139.48	81.60
Line 6	62.37	79.90	139.48	81.60
Line 7	62.37	79.90	298.96	122.80
Line 8	62.37	79.90	141.84	81.80
Line 9	62.37	79.90	142.41	81.60
Line 10	62.37	79.90	244.69	98.10
Line 11	62.37	79.90	141.49	81.80
Line 12	62.37	79.90	140.08	80.99
Line 13	62.37	79.90	144.94	81.88
Line 14	-	-	-	-
Line 15	62.37	79.90	146.46	82.30
Line 16	62.37	79.90	139.42	81.60
Line 17	62.37	79.90	143.67	81.83
Line 18	62.37	79.90	139.49	80.96
Line 19	62.37	79.90	139.50	81.02
Line 20	62.37	79.90	139.82	80.91

For the 14 bus network, island 1 containing bus 2, 3 show similar overload of 62.37 MW, and require load shed of 78.9 MW, the corresponding island 2 an oveload of 139.42 MW to 146.46 MW is recorded on the lines, which requre load in the range of 80.91 MW to 83.6 MW to be shed. Generator 2, and line 2 outage require no island formation as all the buses are grouped as an island. An average overload of 69.23 MW was gotten on island 1 which require an average load shedding of 83.5 MW, and an average load shed of 78.33 MW is required for island 2 from an overload of 143.01 MW.

4.3.4 Load shed speed

The time taken to load shed in both island one and island two as obtained from the simulation result on MATLAB R2013a is given in Table 4.15.

Table 4.15: Time to load shed for IEEE 14 bus

Outage Case	Time to load shed (seconds)	
	Island 1	Island 2
Generator 2	0.0371	-
Generator 3	0.0110	0.0211
Generator 4	0.0111	0.0182
Generator 5	0.0119	0.0170
Line 1	0.0041	0.0176
Line 2	-	0.0323
Line 3	0.0054	0.0197
Line 4	0.0046	0.0135
Line 5	0.0043	0.0171
Line 6	0.0042	0.0161
Line 7	0.0040	0.0191
Line 8	0.0035	0.0159
Line 9	0.0042	0.0167
Line 10	0.0039	0.0191
Line 11	0.0034	0.0221
Line 12	0.0055	0.0168
Line 13	0.0034	0.0212
Line 14	-	-
Line 17	0.0038	0.0158
Line 18	0.0035	0.0217
Line 19	0.0033	0.0164
Line 20	0.0031	0.0174
Total	0.1353	0.3748

From the Table 4.15, an average load shedding time of 0.0068 seconds for island one, and an average load shedding time of 0.0187 seconds for island two was obtained after performing the contingency analysis and load shedding in MATLAB.

The analysis on the 14 bus test system shows that the developed islanding and load shedding scheme can easily be applied on other networks.

4.4 Validation

The result of the developed method was compared with the work of Soman *et al.*,(2015a). The performance metric for the comparison was voltage profile, and load shed speed. The comparison is done on the same test bed of IEEE 6 bus test system. The improved method also showed an improvement over base case average voltage profile by 13.02%.

The Table 4.16 shows the time the developed method and the method of Soman *et al.*,(2015a) takes to load shed in order to obtain stable islands, and the percentage improvement in the time.

Table 4.16: Summary of percentage improvement in load shed speed

Outage	**Developed method (seconds)**	**Soman *et al.*,(2015a) (seconds)**	**Percentage improvement (%)**
Generator 2	0.0132	0.0317	58.3596
Generator 3	0.0113	0.0281	59.7865
Line 1	0.0087	0.0240	63.7500
Line 2	0.0067	0.0207	67.6328
Line 3	0.0074	0.0190	61.0526
Line 4	-	-	-
Line 5	0.0086	0.0213	59.6244
Line 6	0.0068	0.0211	67.7725
Line 7	0.0083	0.0244	65.9836
Line 8	0.0068	0.0221	69.2308
Line 9	0.0092	0.0219	57.9909
Line 10	-	-	-
Line 11	-	-	-
Average	0.0087	0.0234	63.3183

The numerical data of Table 4.16 was obtained after running the contingency analysis, islanding, load shedding and power flow simulation in MATLAB R2013a. an average improvement of 63.3% load shed speed was achieved with the developed scheme with a total average time of 0.0087 seconds, as compared with the method presented by Soman *et al.*, (2015a) having an average time of 0.0234 seconds, this percentage improvement was calculated using equation (3.2) as shown in Table 4.16. the percentage improvement graph is shown on Figures 4.1 and 4.2.

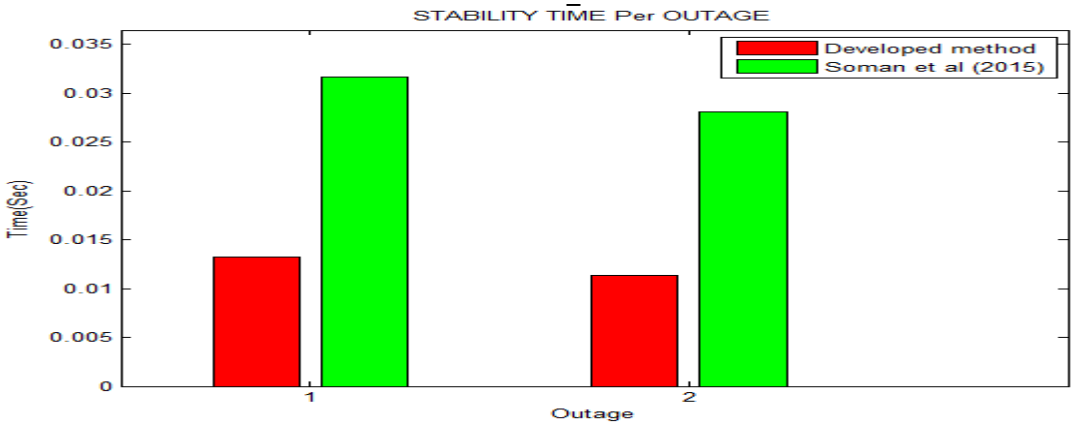


Figure 4.1: Graph of generator outage percentage improvement in load shed speed

It can be seen from Figure 4.1, an improvement of 58.3% load shed speed for generator 2 outage, and improvement of 59.8% speed of load shed for generator 3 outage was gotten over the method of Soman et al. (2015a). The data for plotting the graph was gotten from Table 4.16.

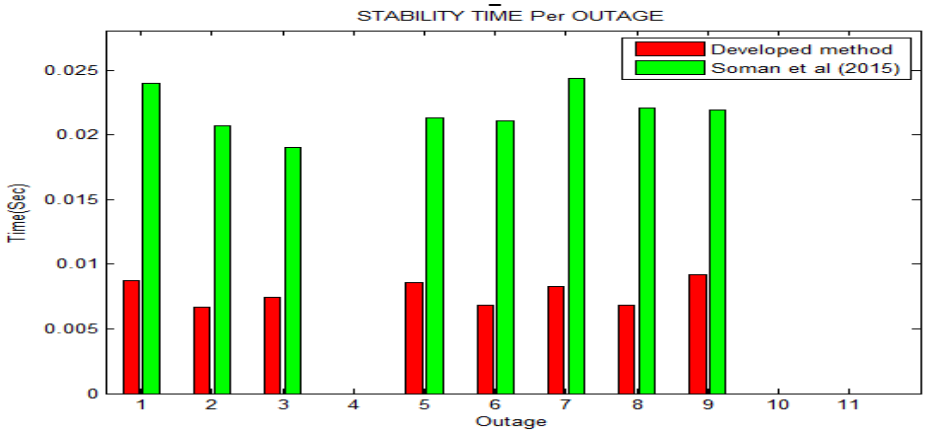


Figure 4.2: Graph of Line outage percentage improvement in load shed speed

The graph of load shedding speed improvement for the eight line outage over the method of Soman et al. (2015a) as presented on Table 4.16. is shown on Figure 4.2.

The average percentage voltage magnitude improvement of the developed method over the method developed by Soman *et al.,* (2015a) for all the outage is given in Table 4.17. The percentage improvement is calculated using equation (3.2). The bus voltage magnitude data is shown in appendix C.

Table 4.17: Voltage Profile Improvement Over Soman et al., (2015a)

Outage	**Voltage Improvement (%)**
Generator 2	1.45
Generator 3	1.74
Line 1	0.32
Line 2	0.24
Line 3	0.82
Line 4	-
Line 5	2.38
Line 6	1.66
Line 7	0.37
Line 8	0.12
Line 9	1.01
Line 10	-
Line 11	-

From the Table 4.17, for the 10 outages that causes violation. After the formation of islands and load shedding, an average voltage improvement of 1.01% was gotten over the method developed by Soman et al., (2015a).

The voltage magnitude of base case, developed method and Soman *et al.*, (2015a) for the 6 bus network ten outages (two generators and eight lines) is shown in Figures 4.3 to 4.12. The numerical data used to plot the graph is contained in appendix C, Tables C1 to C10. this data was obtained after performing the load shedding computation and powerflow analysis on MATLAB software to obtain the results.

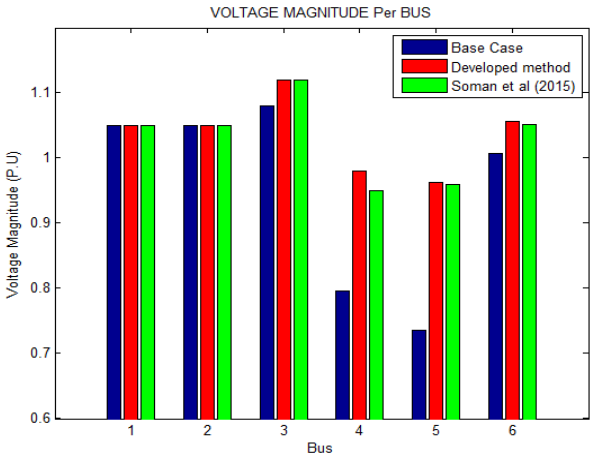


Figure 4.3: Generator 2 Outage

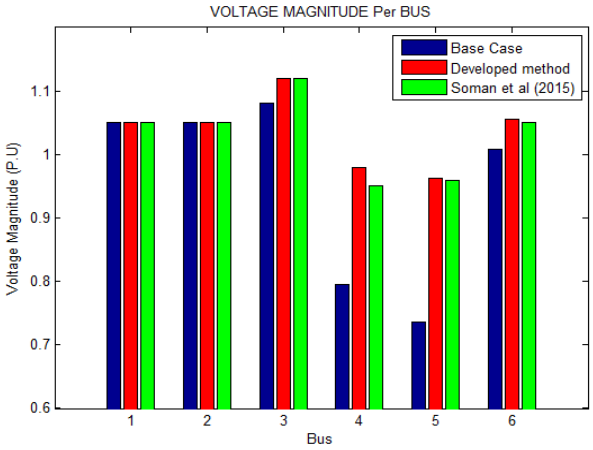


Figure 4.4: Generator 3 Outage

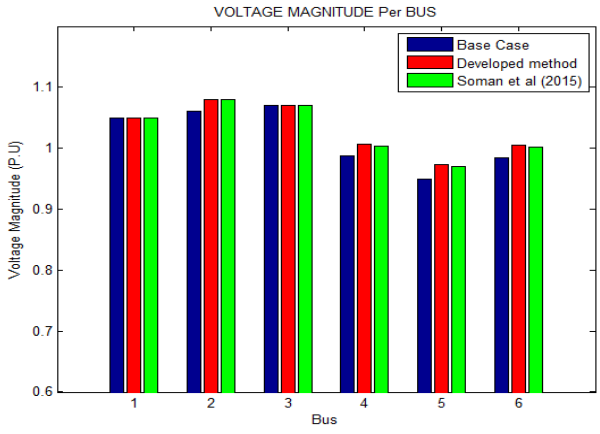


Figure 4.5: Line 1 Outage

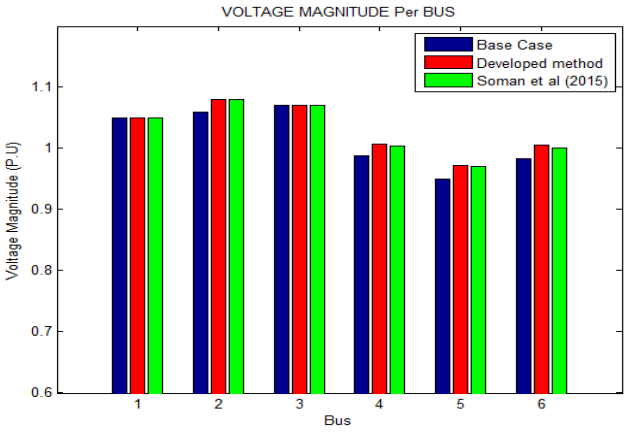


Figure 4.6: Line 2 Outage

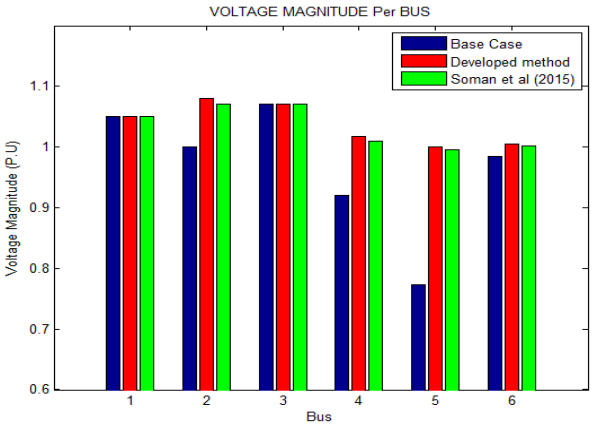


Figure 4.7: Line 3 Outage

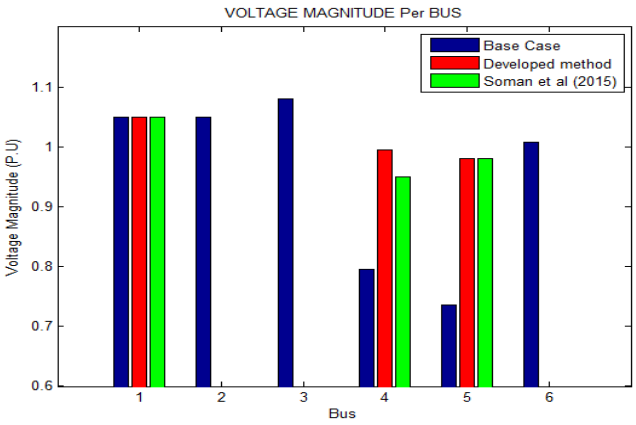


Figure 4.8: Line 5 Outage

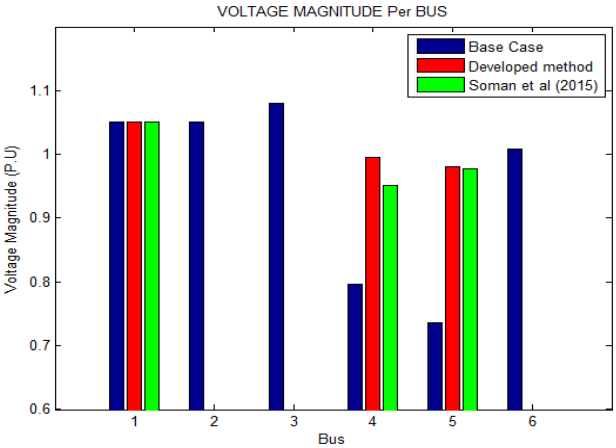


Figure 4.9: Line 6 Outage

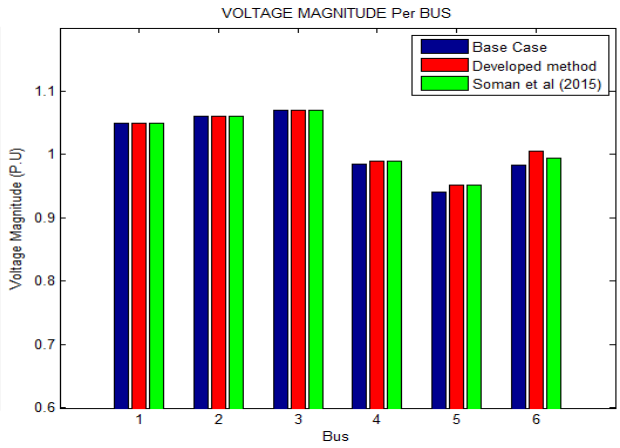


Figure 4.10: Line 7 Outage

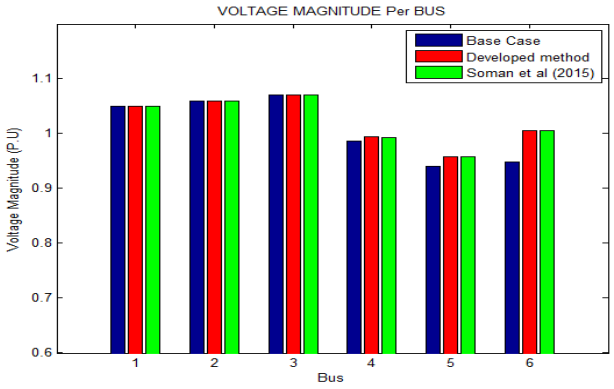


Figure 4.11: Line 8 Outage

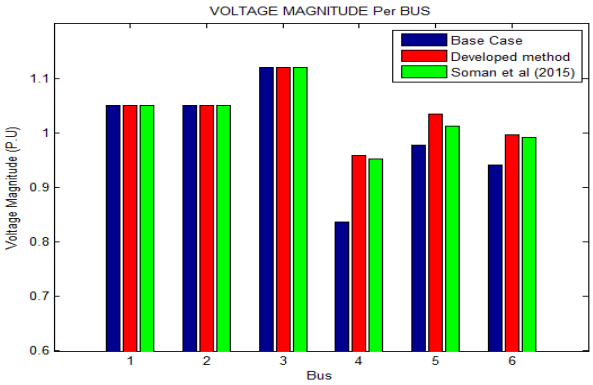


Figure 4.12: Line 9 Outage

From the Figures 4.3 to 4.12, the bus voltage magnitude was violated in the base case while the developed method and Soman *et al.*,(2015a) falls within the acceptable range as defined in subsection (2.2.10) after the load shed.

CHAPTER FIVE

CONCLUSION AND RECOMMENDATIONS

5.1 Introduction

The summary of the research work, conclusion, recommendation and limitation encountered during the course of this research are presented in this chapter. Suggestion for area of future work were presented.

5.2 Conclusion

A forced islanding and load shedding scheme has been developed in order to address contingencies that lead to cascade faults and blackout. This developed scheme ensured the operation of the test system is within the bus voltage safe limit and also a considerable decrease in time of 63.3% was achieved as compared to the method of Soman *et al.*, (2015a) in load shed speed, as verified by the simulation result. The severe contingencies from generator outage and single line outage were obtained from the Active Power Loading Performance Index (APLPI) calculation, and the information was used for the selection of predefined islands, and load shedding strategy. For seek of accuracy, Newton Raphson power flow technique was used for the analysis which give the real power loss of 8.03 MW and reactive power loss of 24.3 MVar. For the load shedding strategy, power imbalance, voltage deviation and line overloads was considered in order to obtain the load to be shed in the islands formed for a stable operation. Two test systems was used in implementing the work, the standard IEEE 6-bus and IEEE 14-bus system. All analysis and plots was carried out on MATLAB R2013a software environment.

5.3 Significant Contribution

The significant contributions of this research work is as follows:

1. Development of an improved predefined island and load shedding scheme to prevent cascade failure that lead to system collapse.

2. The developed method produced an improvement of 1.01% voltage profile, and 63.3% load shed speed improvement over the method of Soman *et al.*,(2015a).

3. The developed method achieved a percentage voltage improvement of 2.89% over the base case for the 14 bus test network.

5.4 Recommendations

1. Load shedding based on load priority can be considered.
2. Double network elements outage (N-2) could be considered for the system contingency analysis on a larger network.

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Appendix A

TABLE A1: Bus data for 6-bus system

Bus No.	Bus Code	Voltage Magnitude	Angle	Generator		Load		Qmax	Qmin
			Degree	MW	MVAR	MW	MVAR	MVAR	MVAR
1	1	1.05	0	0	0	0	0	100	-20
2	2	1.05	0	50	0	0	0	100	-20
3	2	1.05	0	60	0	0	0	100	-20
4	3	1	0	0	0	70	70	0	0
5	3	1	0	0	0	70	70	0	0
6	3	1	0	0	0	70	70	0	0

TABLE A2: Line data for 6-bus system

Line No.	Sending End Bus	Receiving End Bus	Resistance p.u	Reactance p.u	Half Susceptance (p.u)	Power Limit
1	1	2	0.1	0.2	0.02	30
2	1	4	0.05	0.2	0.02	50
3	1	5	0.08	0.3	0.03	40
4	2	3	0.05	0.25	0.03	20
5	2	4	0.05	0.1	0.01	40
6	2	5	0.1	0.3	0.02	20
7	2	6	0.07	0.2	0.025	30
8	3	5	0.12	0.26	0.025	20
9	3	6	0.02	0.1	0.01	60
10	4	5	0.2	0.4	0.04	20
11	5	6	0.1	0.3	0.03	20

Appendix B

TABLE B1: Bus data for 14-bus system

Bus No.	**V (pu)**	**Angle (degree)**	**Pg (MW)**	**Qg (MVAR)**	**Pload (MW)**	**Qload (MVAR)**	**Qmin (MVAR)**	**Qmax (MVAR)**
1	1.060	0.00	114.17	-16.9	0.00	0.00	0.00	10
2	1.045	0.00	40.00	0.00	21.7	12.7	-42.0	50.0
3	1.010	0.00	0.00	0.00	94.2	19.1	23.4	40.0
4	1.000	0.00	0.00	0.00	47.8	3.9	-	-
5	1.000	0.00	0.00	0.00	7.6	1.6	-	-
6	1.000	0.00	0.00	0.00	11.2	7.5	-	-
7	1.000	0.00	0.00	0.00	0.00	0.00	-	-
8	1.000	0.00	0.00	0.00	0.00	0.00	-	-
9	1.000	0.00	0.00	0.00	29.5	16.6	-	-
10	1.000	0.00	0.00	0.00	9.0	5.8	-	-
11	1.000	0.00	0.00	0.00	3.5	1.8	-	-
12	1.000	0.00	0.00	0.00	6.1	1.6	-	-
13	1.000	0.00	0.00	0.00	13.8	5.8	-	-
14	1.000	0.00	0.00	0.00	14.9	5.0	-	-

Table B2: Line data for 14-bus system

Line number	From bus	To bus	R (pu)	X (pu)	Half line charging susceptance (pu)	Rating (MVA)
1	1	2	0.0193	0.0591	0.0264	120
2	1	5	0.0540	0.2230	0.0219	65
3	2	3	0.0469	0.1979	0.0187	36
4	2	4	0.0581	0.1763	0.0246	65
5	2	5	0.0569	0.1738	0.0170	50
6	3	4	0.0671	0.1710	0.0173	65
7	4	5	0.0134	0.0421	0.0064	45
8	4	7	0.0000	0.2091	0.0000	55
9	4	9	0.0000	0.5561	0.0000	32
10	5	6	0.0000	0.2520	0.0000	45
11	6	11	0.0949	0.1989	0.0000	18
12	6	12	0.1229	0.2558	0.0000	32
13	6	13	0.0661	0.1302	0.0000	32
14	7	8	0.0000	0.1761	0.0000	32
15	7	9	0.0000	0.1100	0.0000	32
16	9	10	0.0318	0.0845	0.0000	32
17	9	14	0.1271	0.2703	0.0000	32
18	10	11	0.0820	0.1920	0.0000	12
19	12	13	0.2209	0.1998	0.0000	12
20	13	14	0.1709	0.3580	0.0000	12

Appendix C

Table C1: Generator 2 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0500	1.0500	1.0500	1.0500
3	1.0800	1.1200	1.0800	1.1200
4	0.7957	0.9799	0.7957	0.9506
5	0.7364	0.9632	0.7364	0.9590
6	1.0077	1.0559	1.0077	1.0512

Table C2: Generator 3 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0500	1.0500	1.0500	1.0500
3	1.0800	1.1200	1.0800	1.1200
4	0.7957	0.9949	0.7957	0.9506
5	0.7364	0.9810	0.7364	0.9790
6	1.0077	1.0621	1.0077	1.0585

Table C3: Line 1 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0600	1.0800	1.0600	1.0800
3	1.0700	1.0700	1.0700	1.0700
4	0.9874	1.0069	0.9874	1.0041
5	0.9494	0.9730	0.9494	0.9704
6	0.9841	1.0057	0.9841	1.0015

Table C4: Line 2 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0000	1.1000	1.0000	1.1000
3	1.0700	1.0700	1.0700	1.0700
4	0.8839	1.0529	0.8839	1.0511
5	0.8798	1.0122	0.8798	1.0109
6	0.9841	1.0057	0.9841	1.0015

Table C5: Line 3 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0000	1.0800	1.0000	1.0700
3	1.0700	1.0700	1.0700	1.0700
4	0.9205	1.0168	0.9205	1.0096
5	0.7737	0.9999	0.7737	0.9955
6	0.9841	1.0057	0.9841	1.0015

Table C6: Line 5 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0500	-	1.0500	-
3	1.0800	-	1.0800	-
4	0.7957	0.9949	0.7957	0.9506
5	0.7364	0.9810	0.7364	0.9800
6	1.0071	-	1.0071	-

Table C7: Line 6 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0500	-	1.0500	-
3	1.0800	-	1.0800	-
4	0.7957	0.9949	0.7957	0.9506
5	0.7364	0.9810	0.7364	0.9780
6	1.0077	-	1.0077	-

Table C8: Line 7 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0600	1.0600	1.0600	1.0600
3	1.0700	1.0700	1.0700	1.0700
4	0.9858	0.9902	0.9858	0.9900
5	0.9403	0.9522	0.9403	0.9520
6	0.9841	1.0057	0.9841	0.9950

Table C9: Line 8 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0600	1.0600	1.0600	1.0600
3	1.0700	1.0700	1.0700	1.0700
4	0.9858	0.9937	0.9858	0.9925
5	0.9403	0.9580	0.9403	0.9574
6	0.9483	1.0057	0.94831	1.0048

Table C10: Line 9 Pre and Post Contingency Voltage

	Developed method		Soman et al., (2015a)	
Bus No.	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**	**Pre Load shed Voltage (V)**	**Post Load shed Voltage (V)**
1	1.0500	1.0500	1.0500	1.0500
2	1.0500	1.0500	1.0500	1.0500
3	1.1200	1.1200	1.1200	1.1200
4	0.8365	0.9584	0.8365	0.9523
5	0.9779	1.0353	0.9211	1.0124
6	0.9413	0.9960	0.8716	0.9920

Appendix C1

Calculation on improvement of Voltage Magnitude

From Appendix C, Table C1

Percentage Voltage improvement over base case for Generator 2 outage

At Bus 3: $\left(\frac{1.12-1.08}{1.08}\right)\times 100 = 3.7\%$

At Bus 4: $\left(\frac{0.9799-0.7957}{0.7957}\right)\times 100 = 23.15\%$

At Bus 5: $\left(\frac{0.9632-0.7364}{0.7364}\right)\times 100 = 30.798\%$

At Bus 6: $\left(\frac{1.0559-1.0077}{1.0077}\right)\times 100 = 4.7832\%$

Average percentage improvement: $\left(\frac{3.7+23.15+30.798+4.78}{4}\right) = 15.61\%$

Percentage Voltage improvement over Soman *et al.*, (2015a) case for Generator 2 outage

At Bus 4: $\left(\frac{0.9799-0.9506}{0.9506}\right)\times 100 = 3.0823\%$

At Bus 5: $\left(\frac{0.9632-0.9590}{0.9590}\right)\times 100 = 0.4379\%$

At Bus 6: $\left(\frac{1.0599-1.0512}{1.0512}\right)\times 100 = 0.8276\%$

Average percentage improvement: $\left(\frac{3.0823+0.4379+0.8276}{3}\right) = 1.45\%$

From Appendix C, Table C2

Percentage Voltage improvement over base case for Generator 3 outage

At Bus 3: $\left(\frac{1.12-1.08}{1.08}\right)\times 100 = 3.70\%$

At Bus 4: $\left(\frac{0.9949-0.7957}{0.7957}\right)\times 100 = 20.42\%$

At Bus 5: $\left(\frac{0.9810-0.7364}{0.7364}\right)\times 100 = 33.22\%$

At Bus 6: $\left(\frac{1.0621-1.0077}{1.0077}\right)\times 100 = 5.398\%$

Average percentage improvement: $\left(\frac{3.07+20.42+33.22+5.39}{4}\right) = 15.68\%$

Percentage Voltage improvement over Soman *et al.*, (2015a) case for Generator 3 outage

At Bus 4: $\left(\frac{0.9949-0.9506}{0.9506}\right)\times 100 = 4.66\%$

At Bus 5: $\left(\frac{0.9810-0.9790}{0.9790}\right)\times 100 = 0.204\%$

At Bus 6: $\left(\frac{1.0621-1.0585}{1.0585}\right)\times 100 = 0.3401\%$

Average percentage improvement: $\left(\frac{4.66+0.2043+0.3401}{3}\right) = 1.74\%$

From Appendix C, Table C3

Percentage Voltage improvement over base case for Line 1 outage

At Bus 2: $\left(\frac{1.08-1.06}{1.06}\right)\times 100 = 1.87\%$

At Bus 4: $\left(\frac{1.0069-0.9874}{0.9874}\right)\times 100 = 1.975\%$

At Bus 5: $\left(\frac{0.9730-0.9494}{0.9494}\right)\times 100 = 2.486\%$

At Bus 6: $\left(\frac{1.0057-0.9841}{0.9841}\right)\times 100 = 2.195\%$

Average percentage improvement: $\left(\frac{1.87+1.975+2.489+2.195}{4}\right) = 2.13\%$

Percentage Voltage improvement over Soman *et al.*, (2015a) case for Line 1 outage

At Bus 4: $\left(\frac{1.0069-1.0041}{1.0041}\right)\times 100 = 0.279\%$

At Bus 5: $\left(\frac{0.9730-0.9704}{0.9704}\right)\times 100 = 0.268\%$

At Bus 6: $\left(\frac{1.0057-1.0015}{1.0015}\right)\times 100 = 0.419\%$

Average percentage improvement: $\left(\frac{0.279+0.268+0.419}{3}\right) = 0.322\%$

From Appendix C, Table C4

Percentage Voltage improvement over base case for Line 2 outage

At Bus 2: $\left(\frac{1.1-1.0}{1.0}\right)\times 100 = 0.1\%$

At Bus 4: $\left(\frac{1.0529-0.8839}{0.8839}\right)\times 100 = 19.12\%$

At Bus 5: $\left(\frac{1.0122-0.8798}{0.8798}\right)\times 100 = 15.05\%$

At Bus 6: $\left(\frac{1.0057-0.9841}{0.9841}\right)\times 100 = 2.19\%$

Percentage Voltage improvement over Soman *et al.*, (2015a) case for Line 2 outage

At Bus 4: $\left(\frac{1.0529-1.0511}{1.0511}\right)\times 100 = 0.17\%$

At Bus 5: $\left(\frac{1.0122-1.0109}{1.0109}\right)\times 100 = 0.13\%$

At Bus 6: $\left(\frac{1.0057-1.0015}{1.0015}\right)\times 100 = 0.42\%$

Average percentage improvement: $\left(\frac{0.17+0.13+0.42}{3}\right) = 0.24\%$

Appendix D

m-file: Matlab Code for the developed contingency analysis and load shedding scheme

```
                    m-file: matlab code for the power flow
function[PF_Result, LF_Result]= NewRaph(llined,lbusd,nnbus)
% Program for Newton-Raphson Load Flow Analysis..
% clear all;
% clc;
%%%%%%%%%%%%%%%%%%% WITHOUT CONTIGENCY  %%%%%%%%%%%%%%%%%%%%%
%   REMOVE THE INSERT COMMENT SYMBOL (%) FROM THE NEXT THREE LINES
%     llined=0;
%     lbusd=0;
%     nnbus=0;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% format long;
nbus = ;                   % IEEE-6, IEEE-14..
    if llined==0
        lined = linedatas(nbus);    % Get linedats..
    else lined=llined;
    end
    linedata=lined;
    if lbusd==0
    busd = busdatas(nbus);          % Get busdats..
    else busd=lbusd;
    end
    busdata=busd;
    if nnbus==0
    nbus = nbus;                    % Get nbus..
    else nbus=nnbus;
    end
    nbus;
Y = ybusprgrm(nbus,linedata);         % Calling ybusprgrm.m to get Y-Bus
Matrix..
%busd = busdatas(nbus);     % Calling busdatas..
busd = busdata;
BMva = 100;                % Base MVA..
bus = busd(:,1);           % Bus Number..
type = busd(:,2);          % Type of Bus 1-Slack, 2-PV, 3-PQ..
V = busd(:,3);             % Specified Voltage..
del = busd(:,4);           % Voltage Angle..
Pg = busd(:,5)/BMva;       % PGi..
Qg = busd(:,6)/BMva;       % QGi..
Pl = busd(:,7)/BMva;       % PLi..
Ql = busd(:,8)/BMva;       % QLi..
Qmin = busd(:,9)/BMva;     % Minimum Reactive Power Limit..
Qmax = busd(:,10)/BMva;    % Maximum Reactive Power Limit..
P = Pg - Pl;               % Pi = PGi - PLi..
Q = Qg - Ql;               % Qi = QGi - QLi..
Psp = P;                   % P Specified..
Qsp = Q;                   % Q Specified..
G = real(Y);               % Conductance matrix..
B = imag(Y);               % Susceptance matrix..
pv = find(type == 2 | type == 1);   % PV Buses..
pq = find(type == 3);              % PQ Buses..
npv = length(pv);                  % No. of PV buses..
```

```
npq = length(pq);                    % No. of PQ buses..
Tol = 1;
Iter = 1;
% while (Tol > 1e-5)   % Iteration starting..
    P = zeros(nbus,1);
    Q = zeros(nbus,1);
    % Calculate P and Q
    for i = 1:nbus
        for k = 1:nbus
%                 P(i) = P(i) + V(i)* V(k)*(G(i,k)*cos(del(i)-del(k)) +
B(i,k)*sin(del(i)-del(k)));
%                 Q(i) = Q(i) + V(i)* V(k)*(G(i,k)*sin(del(i)-del(k)) -
B(i,k)*cos(del(i)-del(k)));
%         end
%     end
    % Checking Q-limit violations...
    if Iter <= 7 && Iter > 2    % Only checked up to 7th iterations..
        for n = 2:nbus
            if type(n) == 2
                QG = Q(n)+Ql(n);
                if QG < Qmin(n)
                    V(n) = V(n) + 0.01;
                elseif QG > Qmax(n)
                    V(n) = V(n) - 0.01;
                end
            end
         end
    end
    % Calculate change from specified value
     if Psp(2)>0.40
         Psp=0.40
     end
    P;
    Psp;
    dPa = Psp-P;
    dQa = Qsp-Q;
    k = 1;
    dQ = zeros(npq,1);
    for i = 1:nbus
        if type(i) == 3
            dQ(k,1) = dQa(i);
            k = k+1;
        end
    end
    dP = dPa(2:nbus);
    M = [dP; dQ];       % Mismatch Vector
    % Jacobian
    % J1 - Derivative of Real Power Injections with Angles..
    J1 = zeros(nbus-1,nbus-1);
    for i = 1:(nbus-1)
        m = i+1;
        for k = 1:(nbus-1)
            n = k+1;
            if n == m
                for n = 1:nbus
                    J1(i,k) = J1(i,k) + V(m)* V(n)*(-G(m,n)*sin(del(m)-
del(n)) + B(m,n)*cos(del(m)-del(n)));
```

```
                end
                J1(i,k) = J1(i,k) - V(m)^2*B(m,m);
            else
                J1(i,k) = V(m)* V(n)*(G(m,n)*sin(del(m)-del(n)) -
B(m,n)*cos(del(m)-del(n)));
            end
        end
    end
    % J2 - Derivative of Real Power Injections with V..
    J2 = zeros(nbus-1,npq);
    for i = 1:(nbus-1)
        m = i+1;
        for k = 1:npq
            n = pq(k);
            if n == m
                for n = 1:nbus
                    J2(i,k) = J2(i,k) + V(n)*(G(m,n)*cos(del(m)-del(n)) +
B(m,n)*sin(del(m)-del(n)));
                end
                J2(i,k) = J2(i,k) + V(m)*G(m,m);
            else
                J2(i,k) = V(m)*(G(m,n)*cos(del(m)-del(n)) +
B(m,n)*sin(del(m)-del(n)));
            end
        end
    end
    % J3 - Derivative of Reactive Power Injections with Angles..
    J3 = zeros(npq,nbus-1);
    for i = 1:npq
        m = pq(i);
        for k = 1:(nbus-1)
            n = k+1;
            if n == m
                for n = 1:nbus
                    J3(i,k) = J3(i,k) + V(m)* V(n)*(G(m,n)*cos(del(m)-del(n))
+ B(m,n)*sin(del(m)-del(n)));
                end
                J3(i,k) = J3(i,k) - V(m)^2*G(m,m);
            else
                J3(i,k) = V(m)* V(n)*(-G(m,n)*cos(del(m)-del(n)) -
B(m,n)*sin(del(m)-del(n)));
            end
        end
    end
    % J4 - Derivative of Reactive Power Injections with V..
    J4 = zeros(npq,npq);
    for i = 1:npq
        m = pq(i);
        for k = 1:npq
            n = pq(k);
            if n == m
                for n = 1:nbus
                    J4(i,k) = J4(i,k) + V(n)*(G(m,n)*sin(del(m)-del(n)) -
B(m,n)*cos(del(m)-del(n)));
                end
                J4(i,k) = J4(i,k) - V(m)*B(m,m);
            else
```

```
                J4(i,k) = V(m)*(G(m,n)*sin(del(m)-del(n)) -
B(m,n)*cos(del(m)-del(n)));
            end
        end
    end
    J = [J1 J2; J3 J4];     % Jacobian Matrix.....
%     size(J)
%     size(M)
    X = inv(J)*M;           % Correction Vector
    dTh = X(1:nbus-1);      % Change in Voltage Angle..
    dV = X(nbus:end);       % Change in Voltage Magnitude..
    % Updating State Vectors..
    del(2:nbus) = dTh + del(2:nbus);    % Voltage Angle..
    k = 1;
    for i = 2:nbus
        if type(i) == 3
            V(i) = dV(k) + V(i);        % Voltage Magnitude..
            k = k+1;
        end
    end
    Iter = Iter + 1;
    Tol = max(abs(M));                  % Tolerance..
    V;
end
[PF_Result, LF_Result]=loadflow(nbus,V,del,BMva,llined, lbusd);
% Calling Loadflow.m..
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

            Analysis for generator outage and line outage
clear all;
clc;
tic;
warning 'OFF';
format long;
nbus = 6;                  % IEEE-6, IEEE-14
busd = busdatas(nbus);      % Calling busdatas..
lined = linedatas(nbus);    % Get linedats..
bus = busd(:,1);            % Bus Number..
type = busd(:,2);           % Type of Bus 1-Slack, 2-PV, 3-PQ..
pv = find(type == 2);               % PV Buses..
pq = find(type == 3);               % PQ Buses..
npv = length(pv);                   % No. of PV buses..
npq = length(pq);                   % No. of PQ buses..
nbr = length(lined);                % No. of lines(branches)
sbus = size(busd);
L_lim=(rand(nbr,1))*1e2;            % Creating the line limit, randomly
L_lim=lined(:,7);
n=zeros(nbr,1);                     % creating the number set for each line
for i=1:nbr
    n(i)=i;
 end
%%%%%%%%%%%%  Base case result   %%%%%%%%%%%%%%%%%%
[PF_Result_BC, LF_Result_BC]=NewRaph(0,0,0);
%%%%%%%%%%%%%%%    contigency for line data   %%%%%%%%%%%%%%%%%%%%%%
        for i=1%:nbr
            info=sprintf('THE OUTAGE OF LINE %d ',i);
```

```
            disp(info);
            llined=lined;
            llined(i,:)=[];
            sbusd(11,:)=[];
            rb=11:29;
            sbusd(11:29,1)=rb;
            ssb=size(sbusd);
            lsb=ssb(1);
            %%%
            [PF_Result, LF_Result]=NewRaph(llined,0,0);
            LL_Lim=L_lim;                   % removing the outage line limit
            LL_Lim(i)=[];
            nn=n;                           % romiving the outage line number
            nn(i)=[];
            LLF_Result_BC=LF_Result_BC(:,3);
            LLF_Result_BC(i)=[];
            line_order=[LF_Result(1:end-1,1), LF_Result(1:end-1,2)];
            size(line_order);
            size(nn);
            size(LL_Lim);
            size(LLF_Result_BC(1:end-1));
            BCT_L1=[line_order,nn, LL_Lim,abs(LLF_Result_BC(1:end-
1)),abs(LF_Result(1:end-1,3))];
            %%%%%%%%% APLPI FOR LINE OUTAGE %%%%%%%%%%%%%%%
            m=1;
            w=1/(2*m);
            APR=BCT_L1(:,6)./BCT_L1(:,4); % Ratio active power to power limit
            APRp=APR.^(2*m);
            SI=w*APRp;
            BCT_L2=[BCT_L1,SI];
            overload=BCT_L2(:,4)-BCT_L2(:,6);
                %%%%%%%%%%%  ISLAND FORMATION   %%%%%%%%%%%%%%%%%%%%
                predef=isl_lineO(nbus);
                size_predef=size(predef);
                rrow=size_predef(1);
                ccol=size_predef(2);
                  fibl=1:(ccol/2);
                  sibl=(fibl(end)+1):ccol;
                isl_1_bus=predef(i,fibl);
                isl_2_bus=predef(i,sibl);
                emp1=find(isl_1_bus==0);
                emp2=find(isl_2_bus==0);
                isl_1_bus(emp1)=[];
                isl_2_bus(emp2)=[];
                l_fibl=length(isl_1_bus);
                l_sibl=length(isl_2_bus);
                 %%%%%%%%% BUSDATA FOR ISLAND-one  %%%%%%%%%%%%
                busd_isl_1=zeros(l_fibl,sbus(2));
                for ii=1:l_fibl
                    busd_isl_1(ii,:)=busd(isl_1_bus(ii),:);
                end
                busd_isl_1;
                             if busd_isl_1(1,1)~=1
            ttl_gene=sum(busd_isl_1(:,5));
                    ttl_load=sum(busd_isl_1(:,7));
                    diff=abs(ttl_load-ttl_gene);
                    pow_imb=diff;
```

```
            ldbs=find(busd_isl_1(:,2)==3 | busd_isl_1(:,2)==2);
            t_ldbs=ldbs';
            max_ldbs=max(ldbs);
            pct_load=zeros(max_ldbs,2);
            for ie=t_ldbs
                pct_load(ie,1)=(busd_isl_1(ie,7)/ttl_load)*100;
                pct_load(ie,2)=(busd_isl_1(ie,8)/ttl_load)*100;
            end
            if ttl_gene<=(ttl_load+Asu_ttl_loss*ttl_gene)
                ldsd_pow_imb=diff+Asu_ttl_loss*ttl_gene;
                disp('##########  POWER IMBALANCE ######');
                info=sprintf('Power imbalance = %d',pow_imb);
                disp(info);
            disp('######  LOAD SHED DUE TO POWER IMBALANCE #####');
info=sprintf('Load Shed due to Power imbalance = %d',ldsd_pow_imb);
                disp(info);
            end
            if ttl_gene<=(old_ttl_load+Asu_ttl_loss*ttl_gene)
                for ie=t_ldbs
                    busd_isl_1(ie,7)=(pct_load(ie,1)/100)*ttl_load;
                    busd_isl_1(ie,8)=(pct_load(ie,2)/100)*ttl_load;
                end
   end
            busd_isl_1;
        busd_isl_1_LdSd=busd_isl_1;
        old_busd_isl_1=busd_isl_1;
        nnbus=size_busd_isl_1(1);
        bus_no=1:nnbus;
        new_busd_isl_1=[bus_no busd_isl_1(:,2:end)];
        busd_isl_1=new_busd_isl_1;
        %%%%%%%%% LINEDATA FOR ISLAND-one  %%%%%%%%%%%%
        size_llined=size(llined);
        for ik=1:nbr-1
            for ij=1:l_fibl
                if isl_1_bus(ij)==llined(ik,1)
                    lllined(ik,:)=llined(ik,:);
                end
            end
        end
        lllined;
        ind1=find(lllined(:,1)==0);
        lllined=zeros(size_llined);
        for ik=1:nbr-1
            for ij=1:l_fibl
                if isl_1_bus(ij)==llined(ik,2)
                    lllined(ik,:)=llined(ik,:);
                end
            end
        end
        lllined;
        ind2=find(lllined(:,1)==0);
        ind=[ind1 ; ind2];
        llined;
        llined(ind,:)=[];
        lined_isl_1=llined;
        old_lined_isl_1_no=lined_isl_1;
        o_n_no=[old_busd_isl_1(:,1) bus_no];
```

```
                size_lined_isl_1=size(lined_isl_1);
                no_line=size_lined_isl_1(1);
                for i=1:no_line
                    for j=1:nnbus
                        if lined_isl_1(i,1)==o_n_no(j,1)
                            lined_isl_1(i,1)=o_n_no(j,2);
                        end
                        if lined_isl_1(i,2)==o_n_no(j,1)
                            lined_isl_1(i,2)=o_n_no(j,2);
                        end
                    end
                end
                lined_isl_1;
   [PF_Result_isl_1, LF_Rslt_isl_1]=NewRaph(lined_isl_1, busd_isl_1, nnbus);
                %%%%%%%%% Reordering the bus number to the original %%%%%%%%
                len_onno=length(o_n_no);
                PF_Result_isl_1(1:len_onno,1)=o_n_no(:,1);
                s_old_lined_isl_1_no=size(old_lined_isl_1_no);
                len_oli1=s_old_lined_isl_1_no(1);
                LF_Result_isl_1(1:len_oli1,1:2)=old_lined_isl_1_no(:,1:2);
                %%%%%   Adding the line limit and computing overload   %%%%%
                ori_line=lined;
                l_ol=s_ol(1);
                size_LF_Result_isl_1=size(LF_Result_isl_1);
                slri1=size_LF_Result_isl_1;
                add_col=slri1(1);
                a_c=zeros(add_col,2);
                for ih=1:l_ol
                    for id=1:add_col
                        if lined(ih,1)==LF_Result_isl_1(id,1) &&
lined(ih,2)==LF_Result_isl_1(id,2)
                            a_c(id,1)=lined(ih,7);
                        end
                    end
                end
                a_c;
                n_LF_Result_isl_1=[LF_Result_isl_1 a_c];
                for ik=1:add_col
                    n_LF_Result_isl_1(ik,12)=n_LF_Result_isl_1(ik,11)-
abs(n_LF_Result_isl_1(ik,3));
                end
                n_LF_Result_isl_1;
                LF_Result_isl_1=n_LF_Result_isl_1;
disp('#########################################################');
            disp('----------------------- ISLAND ONE --------------------');
            disp('-----------------------------------------------------');
            disp('         Newton Raphson Loadflow Analysis- island 1 ');
            disp('-----------------------------------------------------');
      disp('| Bus | V | Angle | Injection |  Generation  |     Load  |');
            disp('| No | pu | Degree | MW | MVar | MW | Mvar | MW | MVar |');
            disp('-----------------------------------------------------');
            PF_Result_isl_1
            disp('-----------------------------------------------------');
            disp('        Line FLow and Losses- island 1 ');
            disp('-----------------------------------------------------');
    disp('|From | To | P | Q | From | To | P | Q | Line Loss | Line |Over|');
 disp('| Bus | MW | MVar | Bus | MW | MVar | MW | MVar | Limit |    Load |');
```

```
        disp('------------------------------------------------------');
        LF_Result_isl_1
        disp('------------------------------------------------------');
        tic;
%%%%%%  LOAD SHEDDING -- line contigency -- for island one %%%%%%%%%%
                    %%%%%%%%%  base on line overload  %%%%%
                            ov=over_load;
                            for kl=1:add_col
                                if LF_Result_isl_1(kl,12) < 0
                                    ov(kl,1)=LF_Result_isl_1(kl,2);
        ov(kl,2)=abs(LF_Result_isl_1(kl,12))+LF_Result_isl_1(kl,9);
                                end
                            end
                            ov;
                            szpf=size(PF_Result_isl_1);
                            len_szpf=szpf(1)-1;
                            [qa ws]=(max(ov(:,1)));
                            for zv=ueess:-1:ws
                                if ov(zv,:)==0;
                                    ov(zv,:)=[];
                                end
                            end
                            ov;
                            szov=size(ov);
                            len_ov=szov(1);
                            rdif=len_ov-len_szpf;
                                for xc=1:len_ov;
                                    szov=size(ov);
                                    len_ov=szov(1);
                                    rdif=len_ov-len_szpf;
                                    if rdif>0
                                        if ov(xc,:)==0
                                            ov(xc,:)=[];
                                        end
                                    end
                                end
                            ov(:,2)=(ceil(ov(:,2)));
                            busd_isl_1=busd_isl_1_LdSd;
                            siz_bi1=size(busd_isl_1);
                            len_bi1=siz_bi1(1);
                            for i=1:len_bi1
                                bus_no=ov(i,1);
                                for j=1:len_bi1
                                    if busd_isl_1(j,1)==bus_no,
                                busd_isl_1(j,7)=busd_isl_1(j,7)-ov(i,2);
                                busd_isl_1(j,8)=busd_isl_1(j,8)-ov(i,2);
                                    end
                                end
                            end
                            for tt=1:len_bi1
                                if busd_isl_1(tt,7)<0
                                    busd_isl_1(tt,7)=0;
                                end
                                if busd_isl_1(tt,8)<0
                                    busd_isl_1(tt,8)=0;
                                end
                            end
```

```
                                busd_isl_1;
                                %% pre
                                busd_isl_1(3,7)=0;
                                busd_isl_1(4,7)=0;
                                busd_isl_1(3,8)=70;
                                busd_isl_1(4,8)=70;
                                size_busd_isl_1=size(busd_isl_1);
                                nnbus=size_busd_isl_1(1);
                                 bus_no=1:nnbus;
                                bus_no=bus_no';
                                new_busd_isl_1=[bus_no busd_isl_1(:,2:end)];
                                busd_isl_1=new_busd_isl_1;
                                %%%%%%%% NRPF  %%%%%%%%%%%%
                                [PF_Result_isl_1_ldsd,
            LF_Result_isl_1_ldsd]=NewRaph(lined_isl_1, busd_isl_1, nnbus);
            toc;
            %%%%%%%% Reordering the bus number to the original  %%%%%%%%
                                len_onno=length(o_n_no);
            PF_Result_isl_1_ldsd(1:len_onno,1)=o_n_no(:,1);
               s_old_lined_isl_1_no=size(old_lined_isl_1_no);
                                len_oli1=s_old_lined_isl_1_no(1);
            LF_Result_isl_1_ldsd(1:len_oli1,1:2)=old_lined_isl_1_no(:,1:2);
                   %%%%%%%%%%   Adding the line limit nd computing overload
            %%%%%%%%%%%
                                ori_line=lined;
                                s_ol=size(ori_line);
                                l_ol=s_ol(1);
                     size_LF_Result_isl_1_ldsd=size(LF_Result_isl_1_ldsd);
                                slri1=size_LF_Result_isl_1_ldsd;
                                add_col=slri1(1);
                                a_c=zeros(add_col,2);
                                for ih=1:l_ol
                                    for id=1:add_col
                                  if lined(ih,1)==LF_Result_isl_1_ldsd(id,1)
                           && lined(ih,2)==LF_Result_isl_1_ldsd(id,2)
    [PF_Result_isl_2, LF_Result_isl_2]=NewRaph(lined_isl_2,busd_isl_2,
nnbus);
    %%%%%%%% Reordering the bus number to the original  %%%%%%%%
    len_onno=length(o_n_no);
    PF_Result_isl_2(1:len_onno,1)=o_n_no(:,1);
    s_old_lined_isl_2_no=size(old_lined_isl_2_no);
    len_oli1=s_old_lined_isl_2_no(1);
    LF_Result_isl_2(1:len_oli1,1:2)=old_lined_isl_2_no(:,1:2);
    %%%%%%%%%%   Adding the line limit nd computing overload   %%%%%%%%%%%
    ori_line=lined;
    s_ol=size(ori_line);
    l_ol=s_ol(1);
    size_LF_Result_isl_2=size(LF_Result_isl_2);
    slri1=size_LF_Result_isl_2;
    add_col=slri1(1);
    a_c=zeros(add_col,2);
    for ih=1:l_ol
        for id=1:add_col
            if lined(ih,1)==LF_Result_isl_2(id,1) &&
lined(ih,2)==LF_Result_isl_2(id,2)
                a_c(id,1)=lined(ih,7);
            end
```

```
        end
    end
    a_c;
    n_LF_Result_isl_2=[LF_Result_isl_2 a_c]
    for ik=1:add_col
        n_LF_Result_isl_2(ik,12)=n_LF_Result_isl_2(ik,11)-
abs(n_LF_Result_isl_2(ik,3));
    end
    n_LF_Result_isl_2;
    LF_Result_isl_2=n_LF_Result_isl_2;
tic;
     %%%%%%%%  LOAD SHEDDING -- line contigency -- for island two %%%%%%%%
                      %%%%%%%%  base on line overload  %%%%%
                                over_load=zeros(50,2);
%50 chosen to ensure the number of buses is accomodated- 50 must be greater
than number of buses
                                ov=over_load;
                                for kl=1:add_col
                                    if LF_Result_isl_2(kl,12) < 0
                                        ov(kl,1)=LF_Result_isl_2(kl,2);
ov(kl,2)=abs(LF_Result_isl_2(kl,12))+LF_Result_isl_2(kl,9);
                                    end
                                end
                                ov;
                                szpf=size(PF_Result_isl_2);
                                len_szpf=szpf(1)-1;
                                [qa ws]=(max(ov(:,1)));
                                for zv=ueess:-1:ws
                                    if ov(zv,:)==0;
                                    end
                                end
                                ov;
                                szov=size(ov);
                                len_ov=szov(1);
                                rdif=len_ov-len_szpf;
                                    for xc=1:len_ov;
                                        szov=size(ov);
                                        len_ov=szov(1);
                                        rdif=len_ov-len_szpf;
                                        if rdif>0
                                            if ov(xc,:)==0
                                                ov(xc,:)=[];
                                            end
                                        end
                                    end
                                ov(:,2)=ceil(ov(:,2));
                                busd_isl_2=busd_isl_2_LdSd;
                                siz_bi1=size(busd_isl_2);
                                len_bi1=siz_bi1(1);
                                for i=1:len_bi1
                                    bus_no=ov(i,1);
                                    for j=1:len_bi1
                                        if busd_isl_2(j,1)==bus_no,
                                     busd_isl_2(j,7)=busd_isl_2(j,7)-ov(i,2);
                                     busd_isl_2(j,8)=busd_isl_2(j,8)-ov(i,2);
                                        end
                                    end
```

```
                                end
                                for t=1:len_bi1
                                    if busd_isl_2(t,7)<0
                                        busd_isl_2(t,7)=0;
                                    end
                                    if busd_isl_2(t,8)<0
                                        busd_isl_2(t,8)=0;
                                    end
                                end
                                busd_isl_2;
                                size_busd_isl_2=size(busd_isl_2);
                                nnbus=size_busd_isl_2(1);
                                bus_no=1:nnbus;
                                new_busd_isl_2=[bus_no busd_isl_2(:,2:end)];
                                busd_isl_2=new_busd_isl_2;
                                %%%%%%%%% NRPF  %%%%%%%%%%%%%
[PF_Result_isl_2_ldsd, LF_Rslt_isl_2_ldsd]=NewRaph(lined_isl_2, busd_isl_2,
nnbus);
            toc;
               %%%%%%%%% Reordering the bus number to the original  %%%%%%%%
                                len_onno=length(o_n_no);
                           PF_Result_isl_2_ldsd(1:len_onno,1)=o_n_no(:,1);
                                 s_old_lined_isl_2_no=size(old_lined_isl_2_no);
                                   len_oli1=s_old_lined_isl_2_no(1);
             LF_Result_isl_2_ldsd(1:len_oli1,1:2)=old_lined_isl_2_no(:,1:2);
     %%%%%%%%%%%   Adding the line limit nd computing overload   %%%%%%%%%%%
                                ori_line=lined;
                                s_ol=size(ori_line);
                           size_LF_Result_isl_2_ldsd=size(LF_Result_isl_2_ldsd);
                                slri1=size_LF_Result_isl_2_ldsd;
                                add_col=slri1(1);
                                a_c=zeros(add_col,2);
                                for ih=1:l_ol
                                    for id=1:add_col
                                      if lined(ih,1)==LF_Result_isl_2_ldsd(id,1)
                                   && lined(ih,2)==LF_Result_isl_2_ldsd(id,2)
                                                a_c(id,1)=lined(ih,7);
                                            end
                                    end
                                end
                                a_c;
                             n_LF_Result_isl_2_ldsd=[LF_Result_isl_2_ldsd a_c];
                                  for ik=1:add_col
n_LF_Result_isl_2_ldsd(ik,12)=n_LF_Result_isl_2_ldsd(ik,11)-
abs(n_LF_Result_isl_2_ldsd(ik,3));
                                end
                                n_LF_Result_isl_2_ldsd;
                                LF_Result_isl_2_ldsd=n_LF_Result_isl_2_ldsd;
        end
toc;
%%%%%%%%%%%%%     contigency for generator data    %%%%%%%%%%%%%%%%%%%%%%
tic;
pv=pv';
go=;
for j=pv(go)
    lbusd=busd;
    info=sprintf('THE OUTAGE OF GENERATOR %d ',j);
```

```
    disp(info);
    if lbusd(j,2)==1
        lbusd(j,2)=1;
    else
    lbusd(j,2)=3;
    end
    lbusd(j,[5,6])=0;
    [PF_Result, LF_Result]=NewRaph(0, lbusd,0);
    line_order=[LF_Result(1:end-1,1), LF_Result(1:end-1,2)];
    nn=n;
    LL_Lim=L_lim;
    LLF_Result_BC=LF_Result_BC(:,3);
    BCT_G1=[line_order,nn, LL_Lim,abs(LLF_Result_BC(1:end-
1)),abs(LF_Result(1:end-1,3))];
    %%%%%%%%%%  APLPI FOR GEN OUTAGE  %%%%%%%%%%%%%%%
    m=1;
    w=1/(2*m);
    APR=BCT_G1(:,6)./BCT_G1(:,4)  ;     % Ratio of active power over a line
to the power limit of the line
    APRp=APR.^(2*m);
    SI=w*APRp;
    BCT_G2=[BCT_G1,SI];
    overload=BCT_G2(:,4)-BCT_G2(:,6);
%%%%%%%%%%%%%  ISLAND FORMATION   %%%%%%%%%%%%%%%%%%%%
    predef=isl_genO(nbus);
    size_predef=size(predef);
    rrow=size_predef(1);
    ccol=size_predef(2);
    fibl=1:(ccol/2);                    % fibl- First island bus limit (1-4)
    sibl=(fibl(end)+1):ccol;            % sibl- Second island bus limit (5-8)
    n_row=max(pv);
    ppredef=zeros(n_row, ccol);
    for id=go
        ppredef(j,:)=predef(id,:);
    end
    ppredef;
        isl_1_bus=ppredef(j,fibl);
    isl_2_bus=ppredef(j,sibl);
    emp1=find(isl_1_bus==0);
    emp2=find(isl_2_bus==0);
    isl_1_bus(emp1)=[];
    isl_2_bus(emp2)=[];
    l_fibl=length(isl_1_bus);
    l_sibl=length(isl_2_bus);
    %%%%%%%%%% BUSDATA FOR ISLAND-one  %%%%%%%%%%%%
    busd_isl_1=zeros(l_fibl,sbus(2));
    for ii=1:l_fibl
        busd_isl_1(ii,:)=busd(isl_1_bus(ii),:);
    end
    busd_isl_1;
    otg=find(busd_isl_1(:,1)==j);
    busd_isl_1(otg,5)=0;
    if busd_isl_1(1,1)~=1
    ttl_gene=sum(busd_isl_1(:,5));
    ttl_load=sum(busd_isl_1(:,7));
    old_ttl_load=ttl_load;
    diff=abs(ttl_load-ttl_gene);
```

```
    pow_imb=diff;
    ldbs=find(busd_isl_1(:,2)==3 | busd_isl_1(:,2)==2);
    t_ldbs=ldbs';
    max_ldbs=max(ldbs);
        pct_load=zeros(max_ldbs,2);
    for i=t_ldbs
        pct_load(i,1)=(busd_isl_1(i,7)/ttl_load)*100;
        pct_load(i,2)=(busd_isl_1(i,8)/ttl_load)*100;
    end
    if ttl_gene<=(ttl_load+Asu_ttl_loss*ttl_gene)
        ttl_load=ttl_load-diff-Asu_ttl_loss*ttl_gene;
        ldsd_pow_imb=diff+Asu_ttl_loss*ttl_gene;
        disp('##########  POWER IMBALANCE #########');
        info=sprintf('Power imbalance = %d',pow_imb);
        disp(info);
        disp('######  LOAD SHED DUE TO POWER IMBALANCE ######');
        info=sprintf('Load Shed due to Power imbalance = %d',ldsd_pow_imb);
    %%%%%%%%%% NRPF  %%%%%%%%%%%%%
    [PF_Result_isl_1, LF_Result_isl_1]=NewRaph(lined_isl_1, busd_isl_1,
nnbus);
     %%%%%%%%%% Reordering the bus number to the original  %%%%%%%%
    len_onno=length(o_n_no);
    PF_Result_isl_1(1:len_onno,1)=o_n_no(:,1);
    s_old_lined_isl_1_no=size(old_lined_isl_1_no);
    len_oli1=s_old_lined_isl_1_no(1);
    LF_Result_isl_1(1:len_oli1,1:2)=old_lined_isl_1_no(:,1:2);
    %%%%%%%%%%%%   Adding the line limit nd computing overload   %%%%%%%%%%%%
    ori_line=lined;
    s_ol=size(ori_line);
    l_ol=s_ol(1);
    size_LF_Result_isl_1=size(LF_Result_isl_1);
    slri1=size_LF_Result_isl_1;
    add_col=slri1(1);
    a_c=zeros(add_col,2);
    for ih=1:l_ol
        for id=1:add_col
            if lined(ih,1)==LF_Result_isl_1(id,1) &&
lined(ih,2)==LF_Result_isl_1(id,2)
                a_c(id,1)=lined(ih,7);
            end
        end
    end
    a_c;
    n_LF_Result_isl_1=[LF_Result_isl_1 a_c];
    for ik=1:add_col
        n_LF_Result_isl_1(ik,12)=n_LF_Result_isl_1(ik,11)-
abs(n_LF_Result_isl_1(ik,3));
    end
    n_LF_Result_isl_1;
    LF_Result_isl_1=n_LF_Result_isl_1;
tic;
  %%%%%%%%%%  LOAD SHEDDING -- gen contigency -- for island one %%%%%%%%%%%%%
                                %%%%%%%%%%  base on line overload  %%%%%
                                over_load=zeros(50,2);                      %
50 chosen to ensur all buses are accomodated- 50 greater than number of buses
                                ov=over_load;
                                for kl=1:add_col
```

```
                                    if LF_Result_isl_1(kl,12) < 0
                                        ov(kl,1)=LF_Result_isl_1(kl,2);
ov(kl,2)=abs(LF_Result_isl_1(kl,12))+LF_Result_isl_1(kl,9);
                                    end
                                end
                                ov;
                                ov(:,2)=ceil(ov(:,2));
                                busd_isl_1=busd_isl_1_LdSd;
                                siz_bi1=size(busd_isl_1);
                                len_bi1=siz_bi1(1);
                                for i=1:len_bi1
                                    bus_no=ov(i,1);
                                  for j=1:len_bi1
                                    if busd_isl_1(j,1)==bus_no,
                            busd_isl_1(j,7)=busd_isl_1(j,7)-ov(i,2);
                                   busd_isl_1(j,8)=busd_isl_1(j,8)-ov(i,2);
                                        end
                                    end
                                end
                                for tt=1:len_bi1
                                    if busd_isl_1(tt,7)<0
                                        busd_isl_1(tt,7)=0;
                                    end
                                    if busd_isl_1(tt,8)<0
                                        busd_isl_1(tt,8)=0;
                                    end
                                end
                                busd_isl_1;
                                size_busd_isl_1=size(busd_isl_1);
                                nnbus=size_busd_isl_1(1);
                                bus_no=1:nnbus;
                                bus_no=bus_no';
                                new_busd_isl_1=[bus_no busd_isl_1(:,2:end)];
                                busd_isl_1=new_busd_isl_1;
                        [PF_Result_isl_1_ldsd,
LF_Result_isl_1_ldsd]=NewRaph(lined_isl_1, busd_isl_1, nnbus);
toc;
            %%%%%%%%%% Reordering the bus number to the original  %%%%%%%%
                                len_onno=length(o_n_no);
PF_Result_isl_1_ldsd(1:len_onno,1)=o_n_no(:,1);
s_old_lined_isl_1_no=size(old_lined_isl_1_no);
                                len_oli1=s_old_lined_isl_1_no(1);
    LF_Result_isl_1_ldsd(1:len_oli1,1:2)=old_lined_isl_1_no(:,1:2);
   %%%%%%%%%%%   Adding the line limit nd computing overload   %%%%%%%%%%%
                                ori_line=lined;
                                s_ol=size(ori_line);
                                l_ol=s_ol(1);
size_LF_Result_isl_1_ldsd=size(LF_Result_isl_1_ldsd);
                                slri1=size_LF_Result_isl_1_ldsd;
                                add_col=slri1(1);
                                a_c=zeros(add_col,2);
                                for ih=1:l_ol
                                    for id=1:add_col
                                        if
lined(ih,1)==LF_Result_isl_1_ldsd(id,1) &&
lined(ih,2)==LF_Result_isl_1_ldsd(id,2)
                                            a_c(id,1)=lined(ih,7);
```

```
                                        end
                                    end
                                end
                                a_c;
                                n_LF_Result_isl_1_ldsd=[LF_Result_isl_1_ldsd
a_c];
                                for ik=1:add_col
     n_LF_Result_isl_1_ldsd(ik,12)=n_LF_Result_isl_1_ldsd(ik,11)-
abs(n_LF_Result_isl_1_ldsd(ik,3));
                                end
                                n_LF_Result_isl_1_ldsd;
                                LF_Result_isl_1_ldsd=n_LF_Result_isl_1_ldsd;
    %%%%%%%%% BUSDATA FOR ISLAND-two  %%%%%%%%%%%%
    busd_isl_2=zeros(l_sibl,sbus(2));
    for ii=1:l_sibl
        busd_isl_2(ii,:)=busd(isl_2_bus(ii),:);
    end
    busd_isl_2;
    otg=find(busd_isl_2(:,1)==j);
    busd_isl_2(otg,5)=0;
    if busd_isl_2(1,1)~=1
    ttl_gene=sum(busd_isl_2(:,5));
    ttl_load=sum(busd_isl_2(:,7));
    old_ttl_load=ttl_load;
    diff=abs(ttl_load-ttl_gene);
    pow_imb=diff;
    ldbs=find(busd_isl_2(:,2)==3 |busd_isl_2(:,2)==2);
    t_ldbs=ldbs';
    max_ldbs=max(ldbs);
    pct_load=zeros(max_ldbs,2);
    for i=t_ldbs
        pct_load(i,1)=(busd_isl_2(i,7)/ttl_load)*100;
        pct_load(i,2)=(busd_isl_2(i,8)/ttl_load)*100;
    end
    if ttl_gene<=(ttl_load+Asu_ttl_loss*ttl_gene)
        ttl_load=ttl_load-diff-Asu_ttl_loss*ttl_gene;
        ldsd_pow_imb=diff+Asu_ttl_loss*ttl_gene;
        disp('##################  POWER IMBALANCE ###############');
        info=sprintf('Power imbalance = %d',pow_imb);
        disp(info);
        disp('########  LOAD SHED DUE TO POWER IMBALANCE #########');
        info=sprintf('Load Shed due to Power imbalance = %d',ldsd_pow_imb);
        disp(info);
    end
    if ttl_gene<=(old_ttl_load+Asu_ttl_loss*ttl_gene)
        for i=t_ldbs
            busd_isl_2(i,7)=(pct_load(i,1)/100)*ttl_load;
            busd_isl_2(i,8)=(pct_load(i,2)/100)*ttl_load;
        end
    end
    end
    busd_isl_2_LdSd=busd_isl_2;
    old_busd_isl_2=busd_isl_2;
    size_busd_isl_2=size(busd_isl_2);
    nnbus=size_busd_isl_2(1);
    bus_no=1:nnbus;
    bus_no=bus_no';
```

```
    new_busd_isl_2=[bus_no busd_isl_2(:,2:end)];
    busd_isl_2=new_busd_isl_2;
    %%%%%%%%%% LINEDATA FOR ISLAND-two  %%%%%%%%%%%%
    llined=lined;
    size_llined=size(llined);
    lllined=zeros(size_llined);
    for ik=1:nbr-1
        for ij=1:l_sibl
            if isl_2_bus(ij)==llined(ik,1)
                lllined(ik,:)=llined(ik,:);
            end
        end
    end
    lllined;
    ind1=find(lllined(:,1)==0);
    lllined=zeros(size_llined);
    for ik=1:nbr-1
        for ij=1:l_sibl
            if isl_2_bus(ij)==llined(ik,2)
                lllined(ik,:)=llined(ik,:);
            end
        end
    end
    ind2=find(lllined(:,1)==0);
    ind=[ind1 ; ind2];
    llined;
    o_n_no=[old_busd_isl_2(:,1) bus_no];
    size_lined_isl_2=size(lined_isl_2);
    no_line=size_lined_isl_2(1);
    for i=1:no_line
        for j=1:nnbus
            if lined_isl_2(i,1)==o_n_no(j,1)
                lined_isl_2(i,1)=o_n_no(j,2);
            end
            if lined_isl_2(i,2)==o_n_no(j,1)
                lined_isl_2(i,2)=o_n_no(j,2);
            end
        end
    end
    lined_isl_2;
   %%%%%%%%%% NRPF  %%%%%%%%%%%%%
   [PF_Result_isl_2, LF_Result_isl_2]=NewRaph(lined_isl_2,busd_isl_2, nnbus);
   %%%%%%%%%% Reordering the bus number to the original  %%%%%%%%
    len_onno=length(o_n_no);
    PF_Result_isl_2(1:len_onno,1)=o_n_no(:,1);
    s_old_lined_isl_2_no=size(old_lined_isl_2_no);
    LF_Result_isl_2(1:len_oli1,1:2)=old_lined_isl_2_no(:,1:2);
    %%%%%%%%%%%%   Adding the line limit nd computing overload   %%%%%%%%%%%%
    ori_line=lined;
    s_ol=size(ori_line);
    l_ol=s_ol(1);
        size_LF_Result_isl_2=size(LF_Result_isl_2);
    a_c=zeros(add_col,2);
    for ih=1:l_ol
        for id=1:add_col
            if lined(ih,1)==LF_Result_isl_2(id,1) &&
lined(ih,2)==LF_Result_isl_2(id,2)
```

```
                a_c(id,1)=lined(ih,7);
            end
        end
    end
    a_c;
    n_LF_Result_isl_2=[LF_Result_isl_2 a_c];
    for ik=1:add_col
        n_LF_Result_isl_2(ik,12)=n_LF_Result_isl_2(ik,11)-
abs(n_LF_Result_isl_2(ik,3));
    end
    n_LF_Result_isl_2;
    LF_Result_isl_2=n_LF_Result_isl_2;
disp('#####################################################################');
disp('-------------------------- ISLAND TWO ----------------------------');
disp('                              Newton Raphson Loadflow Analysis ');
disp('--------------------------------------------------------------------');
disp('| Bus     |    V      |  Angle  |     Injection      |     Generation
|          Load      |');
disp('| No      |   pu      |  Degree |    MW   |   MVar   |    MW   |  Mvar
|     MW     |  MVar |');
disp('--------------------------------------------------------------------');
PF_Result_isl_2
disp('                              Line FLow and Losses ');
disp('-----------------------------------------------------------------');
disp('  |From |     To      |    P    |    Q     | From     | To    |    P
|   Q     |   Line Loss    |   Line  |    Over    |');
disp('  |Bus  |     Bus     |   MW    |   MVar   | Bus      | Bus   |    MW
|  MVar   |  MW   |   MVar |   Limit |    Load    |');
disp('-----------------------------------------------------------------');
tic;
  %%%%%%%%%%  LOAD SHEDDING -- gen contigency -- for island two %%%%%%%%%%%%%
                              %%%%%%%%%  base on line overload  %%%%%
                              over_load=zeros(50,2);                          %
50 chosen to ensure the number of buses is accomodated- 50 must be greater
than number of buses
                              ov=over_load;
                              for kl=1:add_col
                                  if LF_Result_isl_2(kl,12) < 0
                                      ov(kl,1)=LF_Result_isl_2(kl,2);
      ov(kl,2)=abs(LF_Result_isl_2(kl,12))+LF_Result_isl_2(kl,9);
                                  end
                              end
                              ov;
                              ov(:,2)=ceil(ov(:,2)).*0.9;
                              busd_isl_2=busd_isl_2_LdSd;
                              len_bi1=siz_bi1(1);
                              for i=1:len_bi1
                                  bus_no=ov(i,1);
                                  for j=1:len_bi1
                                      if busd_isl_2(j,1)==bus_no,
                                          busd_isl_2(j,7)=busd_isl_2(j,7)-
ov(i,2);
                                          busd_isl_2(j,8)=busd_isl_2(j,8)-
ov(i,2);
                                      end
                                  end
                              end
```

```
                                busd_isl_2;
                                size_busd_isl_2=size(busd_isl_2);
                                nnbus=size_busd_isl_2(1);
                                bus_no=1:nnbus;
                                new_busd_isl_2=[bus_no busd_isl_2(:,2:end)];
                                busd_isl_2=new_busd_isl_2;
                                %%%%%%%%%% NRPF  %%%%%%%%%%%%%
                                          [PF_Result_isl_2_ldsd,
            LF_Result_isl_2_ldsd]=NewRaph(lined_isl_2, busd_isl_2, nnbus);
            toc;
              %%%%%%%%%% Reordering the bus number to the original  %%%%%%%%
                                len_onno=length(o_n_no);
      PF_Result_isl_2_ldsd(1:len_onno,1)=o_n_no(:,1);
                                len_oli1=s_old_lined_isl_2_no(1);
  LF_Result_isl_2_ldsd(1:len_oli1,1:2)=old_lined_isl_2_no(:,1:2);
   %%%%%%%%%%%   Adding the line limit nd computing overload   %%%%%%%%%%%
                                ori_line=lined;
size_LF_Result_isl_2_ldsd=size(LF_Result_isl_2_ldsd);
                                slri1=size_LF_Result_isl_2_ldsd;
                                a_c=zeros(add_col,2);
                                for ih=1:l_ol
                                    for id=1:add_col
                                        if
lined(ih,1)==LF_Result_isl_2_ldsd(id,1) &&
                                            a_c(id,1)=lined(ih,7);
                                        end
                                    end
                                end
                                a_c;
                                n_LF_Result_isl_2_ldsd=[LF_Result_isl_2_ldsd
a_c];
                                for ik=1:add_col
n_LF_Result_isl_2_ldsd(ik,12)=n_LF_Result_isl_2_ldsd(ik,11)-
abs(n_LF_Result_isl_2_ldsd(ik,3));
                                end
                                LF_Result_isl_2_ldsd=n_LF_Result_isl_2_ldsd;
disp('##################################################################');
         disp('--------------  LOAD SHED in ISLAND TW0  -----------------');
         disp(' Newton Raphson Loadflow Analysis- island 1 ');
                             disp('-----------------');
 disp('| Bus     |    V      |  Angle  |     Injection      |     Generation
|          Load      |');
                             disp('| No      |   pu      |  Degree |    MW   |
MVar   |    MW   |  Mvar    |     MW     |  MVar |');
         disp('-----------------------------------------------');
                             PF_Result_isl_2_ldsd
         disp('-----------------------------------------------');
        disp(' Line FLow and Losses- island 1 ');
       disp('-------------------------------------------------');
       disp('  |From |     To      |    P    |    Q     | From     | To    |
P     |   Q     |   Line Loss    |   Line  |    Over    |');
                             disp('  |Bus  |     Bus     |   MW    |   MVar
| Bus      | Bus   |    MW    |  MVar   |  MW   |   MVar |   Limit |    Load
|');
            LF_Result_isl_2_ldsd
        disp('-------------------------------------------------------------');
end
```